Partners:
OUL, IMEC, LMF, SEQ, NGE, WIN, ORA, SAT, EAB, AAU, QLC, SON, BI, TUD, NXP

HEXA-X-II D5.5 Deliverable

Final design of enabling technologies for 6G devices and infrastructure

Hexa-X-II

hexa-x-ii.eu

01.03.2025

Deliverable structure

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8. Conclusions

Appendices

2. Device Classes

- Sensing Analysis
- Use-cases and Device Classes with Example Devices
- Device Classes Updates: Main Takeaways

Sensing Analysis

Sensing approach	Impact on devices and NW	Potential device classes
UE - sensing (monostatic)	Devices sense and process on their own for collision detection, localization, navigation etc.	RHDRBL , HRLL
UE - assisted sensing	Network provides fully or partially processed sensing information Devices may or may not have sensing capability.	EN, RHDRBL, HRLL
UE - collaborative sensing (mono-, bi-, multi-static)	Sends UE's own sensing raw or pre-processed data (may or may not use its own sensing data). Network or peers with processing capability will act/forward. Might request processed or data fused sensing data.	RHDRB , HRLL (if it is within acceptable latency)
UE - "Sensing Network Function"	Networks implement "Sensing/Radar" as network function. Network may broadcast or multicast its NF -Sensing capabilities. Devices to request sensing information. NF can provide enhanced sensing data like object tracking and motion estimates (could be AI assisted)	RHDRBL, HRLL, eLPWA
UE - sensing - AAA	Device and network may have additional or improved service agreement for Authentication, Authorization & Accounting (AAA) for sensing or radar services/features.	RHDRBL, HRLL, eLPWA

Main takeaways:

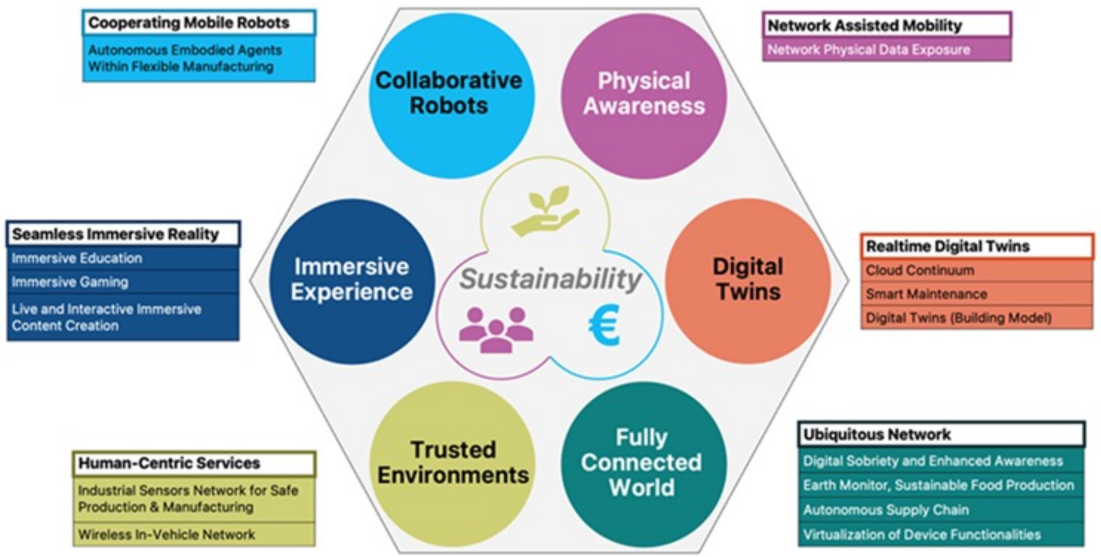
- Different **sensing approaches analyzed** with **device and NW roles** along with **device classes mapping.**
- **JCAS:** No dedicated device class (rather an additional feature - inline with D5.2 assumptions)

Device classes (identified in D5.2)

EN : Energy Neutral
RHDRBL : Reliable High Data Rate with Bounded Latency
HRLL : High Reliability and Low latency
eLPWA : enhanced Low Power Wide Area
EURLLC : Enhancements of URLLC
feMBB : further enhanced MBB

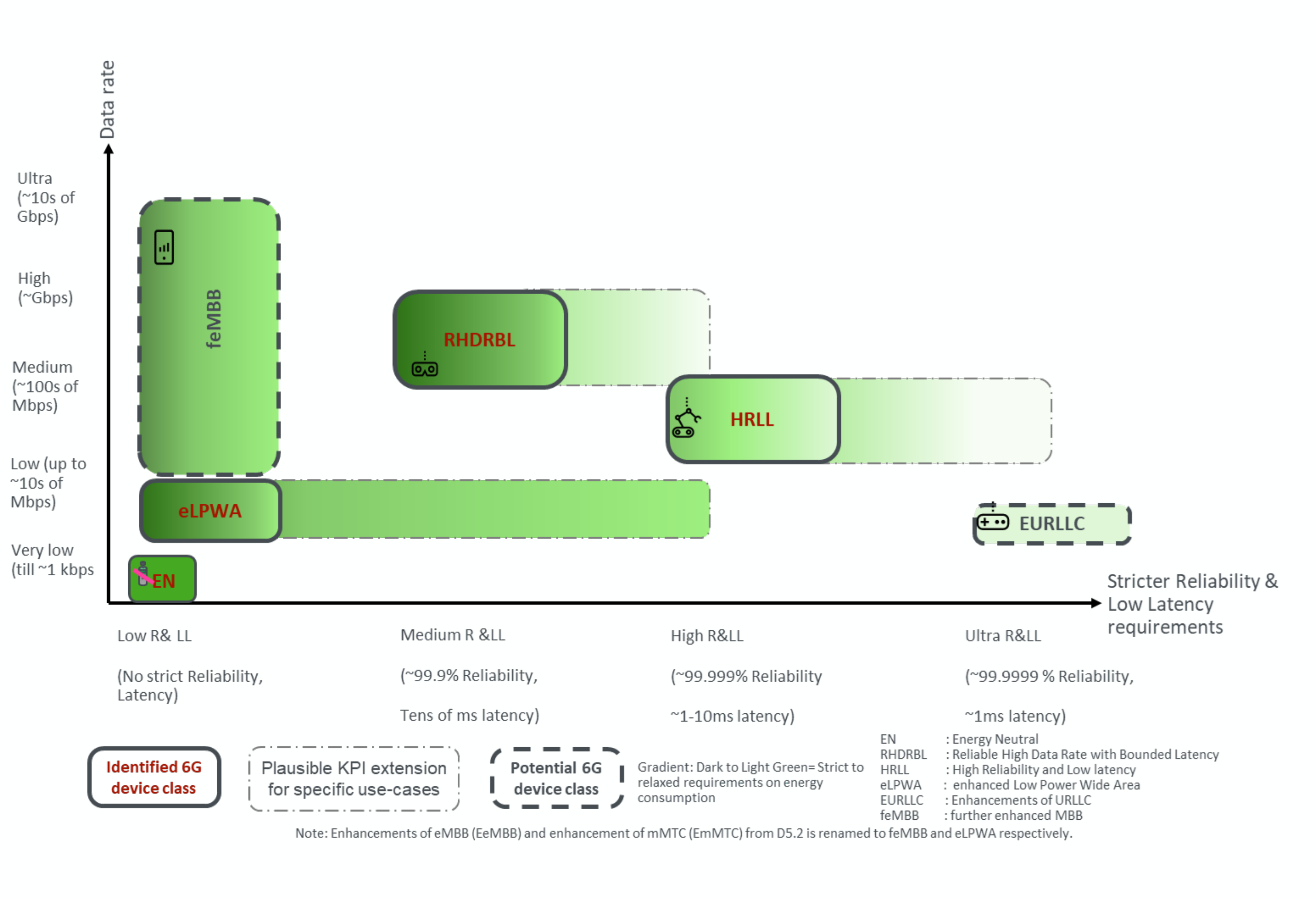
Note: Enhancements of eMBB (EeMBB) and enhancement of mMTC (EmMTC) from D5.2 is renamed to feMBB and eLPWA respectively.

Use-cases and Device Classes with Example Devices



Device Class	Key use cases served	Example devices
Energy Neutral (EN)	Realtime Digital Twins, Ubiquitous Network, Human-Centric Services	Sensors, Tags/stickers
Reliable High Data Rate with Bounded Latency (RHDRBL)	Seamless Immersive Reality	AR glasses, VR headsets
Highly Reliable and Low latency (HRLL)	Cooperative mobile robots	Cooperative mobile robots, IIoT devices, …
Enhanced Low Power Wide Area (eLPWA)	Ubiquitous Network, Realtime Digital Twins, Network-Assisted Mobility	Meters, Trackers, Sensors, Wearables, Smart devices

Device Classes Updates: Main Takeaways



- More than one device needed to realize a use-case
- Economies of scale is important for adoption of a device class.
- Still *four main novel device classes in 6G* (as identified in D5.2) but some of them may have soft upper bounds on KPI to realize a specific use-case
- Sensing is feature that could be suitable for most device classes, could be adopted based on the available device capabilities (for e.g., compute, energy source)

3. FR1/FR2/FR3 Transceivers

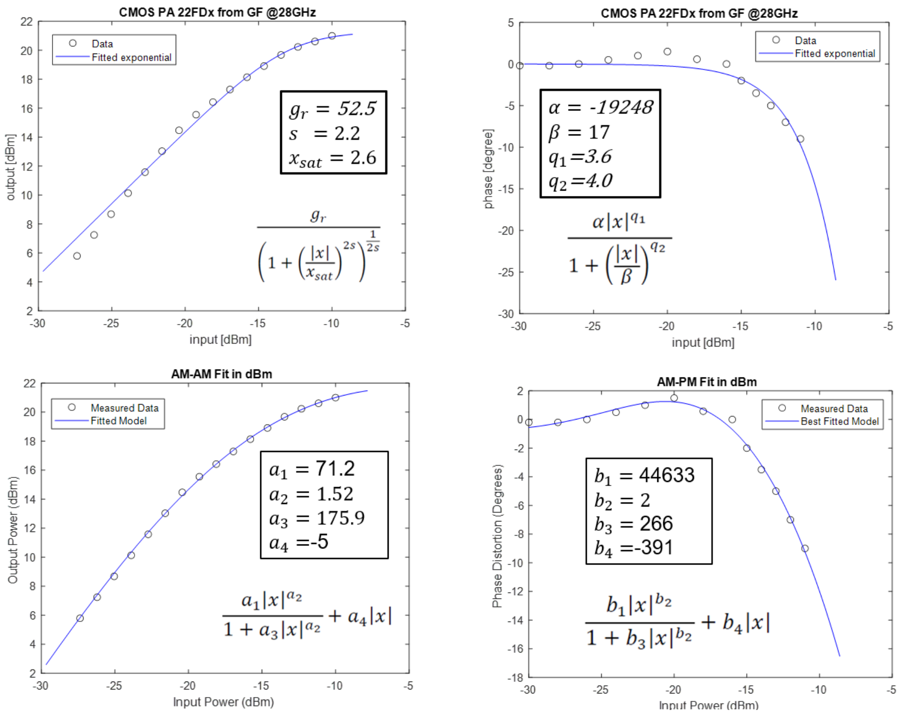
- Updated PA Models in FR2/FR3
  - Better non-linearity fit from Ghorbani than Rapp models; FR3 may also use III/V technos (such as GaN) at UE side
- Review of 5G NCR Standardization by 3GPP for RIS
  - Some similarities between NCR and RIS but could constrain RIS design
- Test Results of the FR2 RIS Prototype (16x16 tile)
  - Calibration Principle
  - Performances
- FR3 UE Power Constraints due to EMF Compliance Limits
  - The time-averaged power and EIRP that can be achieved by FR3 UE are derived.
- Low-complexity DFT-s-OFDM Transmission
  - Replacing FFT-mapping-IFFT by filter allows complexity reduction trade-offs

Updated PA Models & NCR Standardization for RIS

- FR2 PA models: CMOS vs. III/V technos
  - Rapp and Ghorbani model fits for AM and PM distortion (CMOS case for UE)

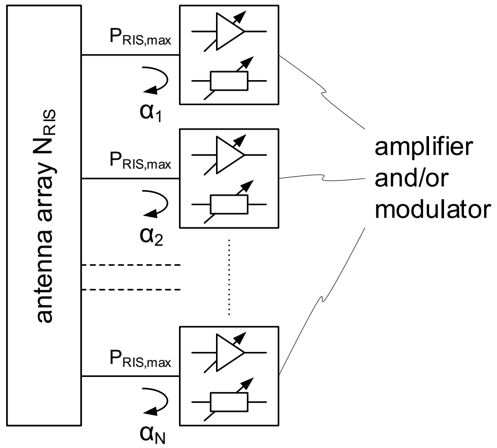
Rapp

Ghorbani



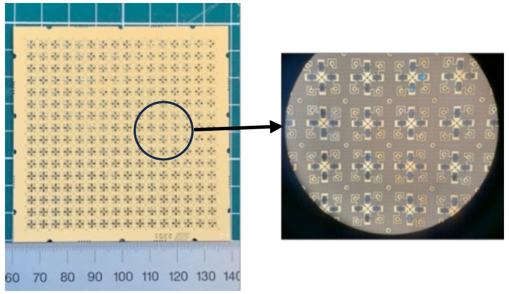
- FR3 UEs may include advanced PA topologies and technos (GaN vs. GaAs)

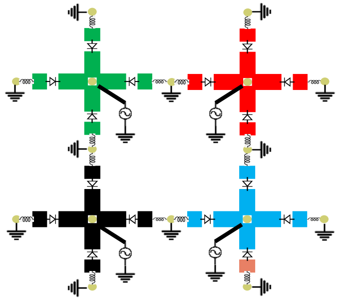
- Review of NCR standardization for RIS
  - RIS have fundamentally different architecture for relaying signals compared to NCR.
  - Most requirements are applicable
  - Specification of the out-of-band gain needs a technical clarification for RIS.
  - With current RIS technology this parameter can cause a limitation in the RIS design.



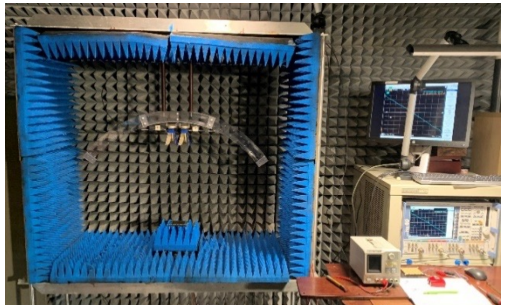
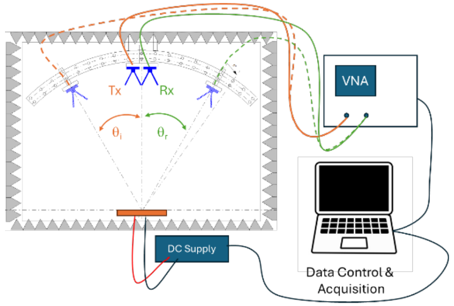
Test Results of the FR2 RIS Prototype (16x16 tile)

- RIS Calibration:
  - (reflection coefficient vs applied voltage) rule



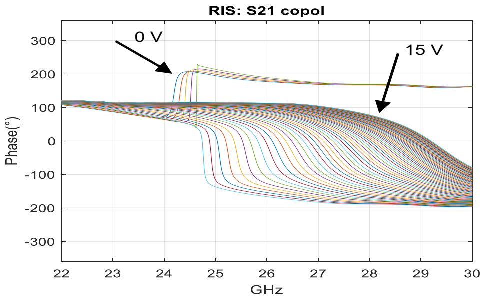


  - Same voltage applied on all the 256 cells
  - Transmission between two horns via the RIS

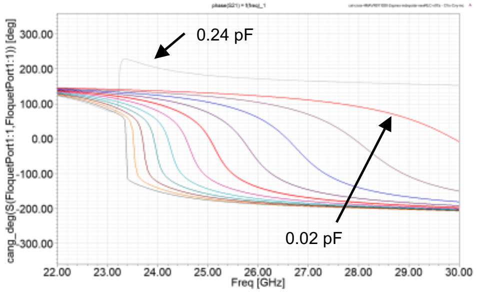



  - Depending:
    - Incidence angle
    - Incident field polarization

- Results:
  - Good agreement with simulations:
    - Frequency offset ~ 1 GHz

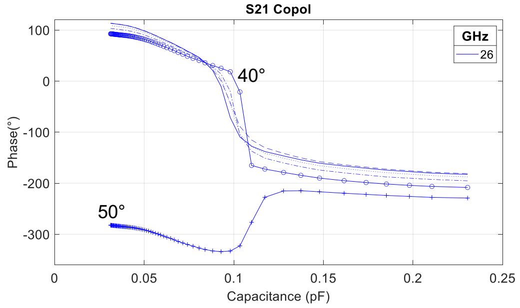


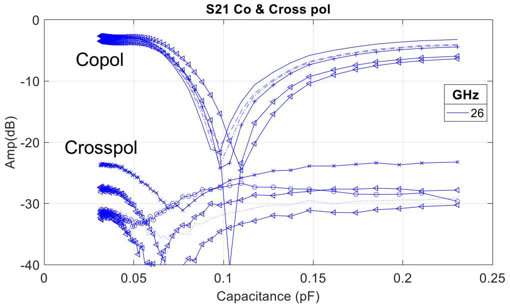
experiments



Simulations

  - RIS performance:
    - 300° of phase control as expected
      - Up to 50° of incidence
    - Cross-polarization isolation > 17 dB

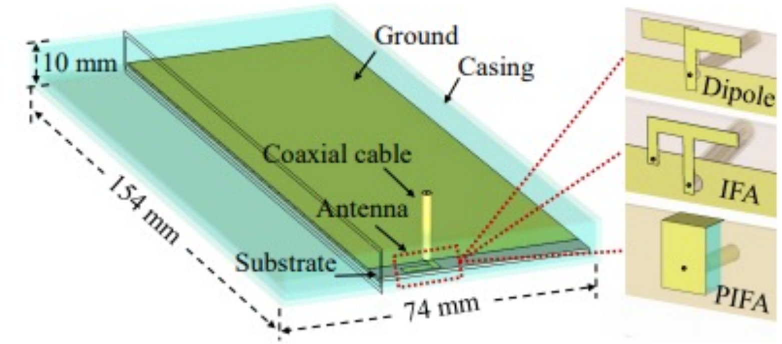




UE Power Constraints and Low-complexity DTF-s-OFDM

- FR3 UE power constraints due to EMF exposure limits

- For a UE operating above 6 GHz, the absorbed power density, with a limit value of 20 W/m^2, is used to determine EMF compliance according to the ICNIRP guidelines published in 2020.
- The absorbed power density levels for a handheld UE mock-up are evaluated across the 6–15 GHz spectrum. Various single-antenna designs are analysed. Additionally, dual-antenna placements are considered for both correlated and uncorrelated combining in EMF assessments.
- The maximum allowed time-averaged power accepted by the antenna and the resulting maximum time-averaged EIRP levels are computed.



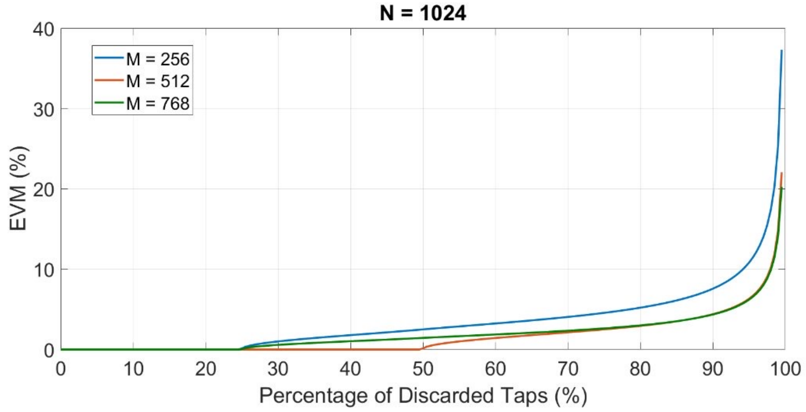
- **Low-complexity DTF-s-OFDM**

Traditional DFTS-OFDM transmitter requires one DFT and one IDFT.

- **Challenges:**
  - High computational complexity and increased power consumption
- **Proposed Idea:**
  - A **time-domain filter** is designed to represent the sequence of DFT, subcarrier mapping, and IDFT.
    - The filter response will be shortened to reduce the complexity at the cost of signal distortion

$$\boldsymbol{y} = \boldsymbol{F}_N^{-1}\boldsymbol{P}\boldsymbol{F}_M\boldsymbol{x} = \boldsymbol{A}\boldsymbol{x} \longrightarrow \tilde{\boldsymbol{y}} = \tilde{\boldsymbol{A}}\,\boldsymbol{x}$$

- The properties of time-domain filter were investigated for various parameters including DFT size, IDFT size, QAM order, etc.

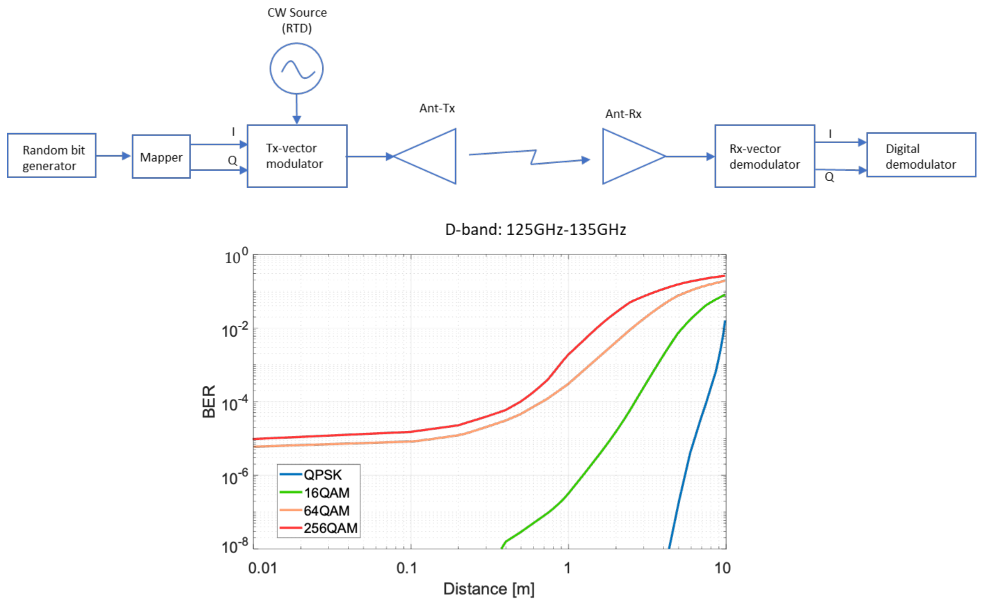


4. Sub-THz Transceivers

- Performance of RTD-based Devices
  - 34m radio link distance using QPSK and 10m radio link using 256QAM (for a 4x4 RTD+antenna array)
- Dimensioning Trade-offs for Energy Efficiency
  - Digital power consumption lower than analogue power in most cases
- Updated sub-THz Non-ideality Models including PA
  - Best PA designs achieve 22-27 dBm Psat and 18-33% PAE
  - Impact of PAs with memory limited to region with high BW, high BO and low EVM
- Sub-THz Antenna Array Integration
  - Irregular arrays solve half-wavelength spacing constraints while trading off beamforming gain vs. side-lobes
- LO Delay-based Wideband PN Mitigation
  - Delay difference helps to reduce wideband phase noise in array level by creating nulls to the combined phase noise spectrum.
  - Also delay can help to reduce the impact of phase noise in monostatic sensing.

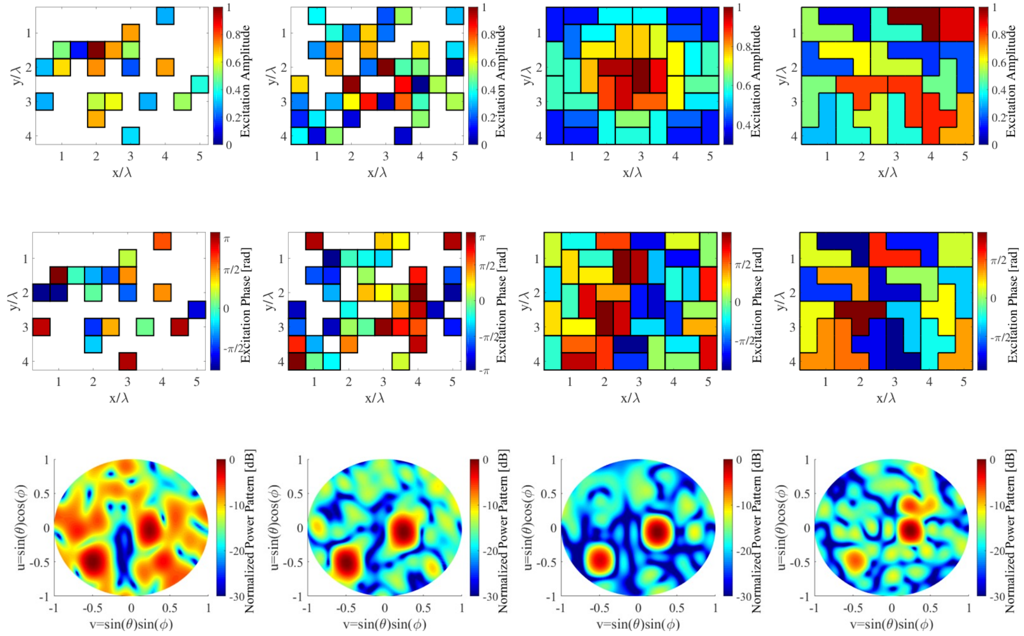
RTD-based Devices & Antenna Array Integration

- RTD-based devices



- The performance of a Tx-Rx D-band (140GHz) using RTD is assessed for different modulation formats and communication distances
- NF at the receiver and Tx phase phase noise at different carrier offsets have been included in the simulation scenario
- 1-elem RTD-antenna, 2x2 and 4x4 RTD-antenna array architectures have been simulated
- higher order modulation formats are more sensitive to the nonlinearity effects, and as such provide shorter distance links compared to simpler formats (34m radio link distance using QPSK (for BER=10^{-6}) and 10m radio link with 256QAM (for a BER=10^{-2} for a 4x4 RTD-antenna array)

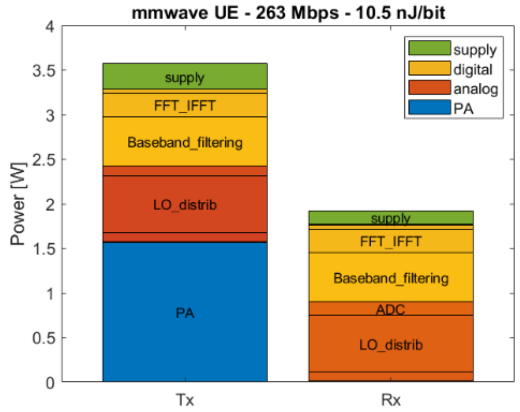
- Irregular antenna array solutions
  - Half-wavelength spacing relaxed
  - No strong grating lobes
  - Trade-off beam gain vs. side-lobes



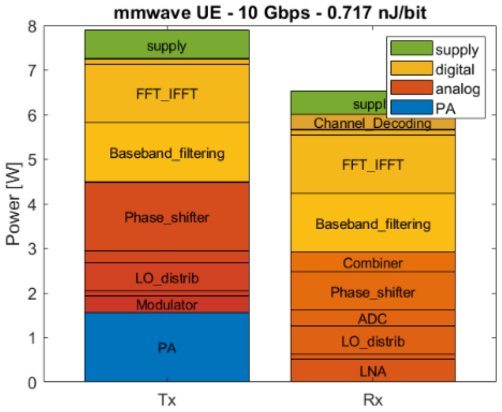
Dimensioning Trade-offs for Energy Efficiency

- Power consumption dominance: analogue (low-bandwidth) vs. digital (high-bandwidth) depending on use case (64 antennas, single-stream UE, 5 bps/Hz), architecture, technology (optimized CMOS in older 20nm or recent 3nm)
- Analogue power dominates until a bandwidth of:
  - Full-digital: 60 MHz (old CMOS) or 1.1 GHz (recent CMOS)
  - Hybrid partially-connected (4 RF chains): 2.3 GHz (old) or > 30 GHz (recent)
  - Analogue beamforming: 11 GHz (old) or > 30 GHz (recent)

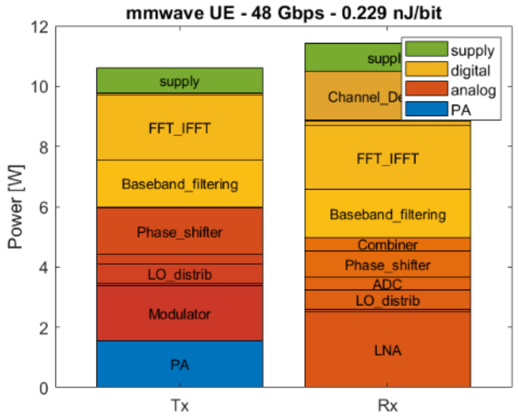
FD



HPC



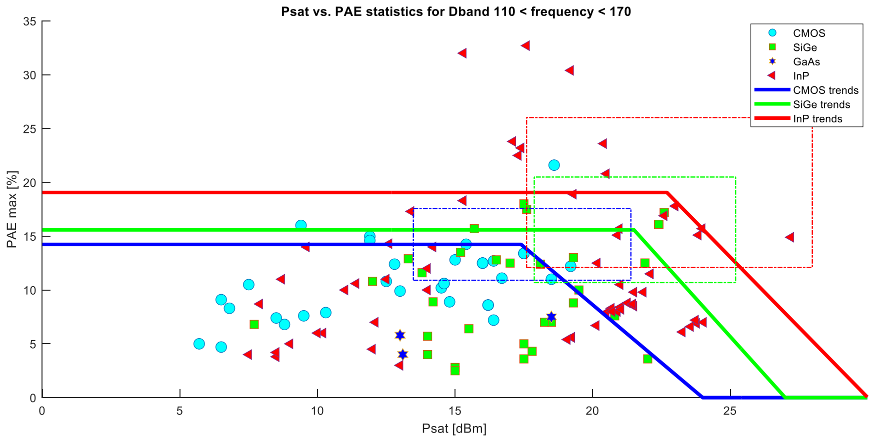
ABF



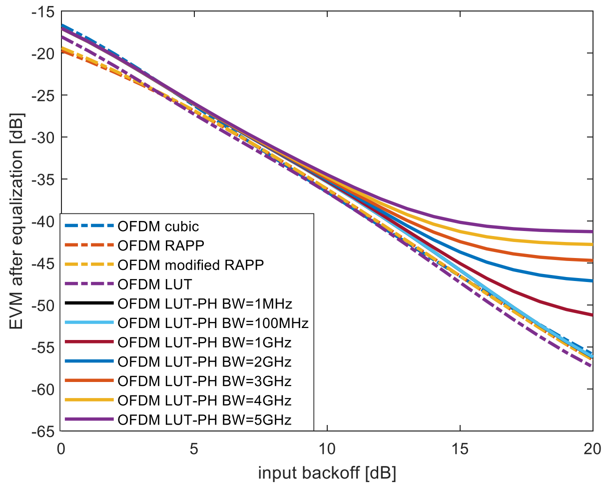
- Hence an efficient digital implementation will consume a limited share of the power
  - Advanced digital power reduction (such as 1-bit ADC) might not be necessary

Updated Sub-THz Non-ideality Models including PA

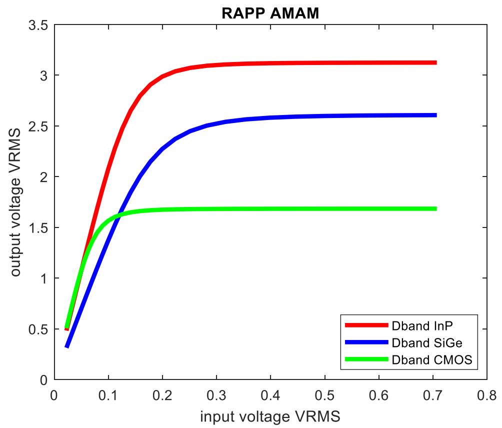
- Trends in output power and efficiency updated from recent designs

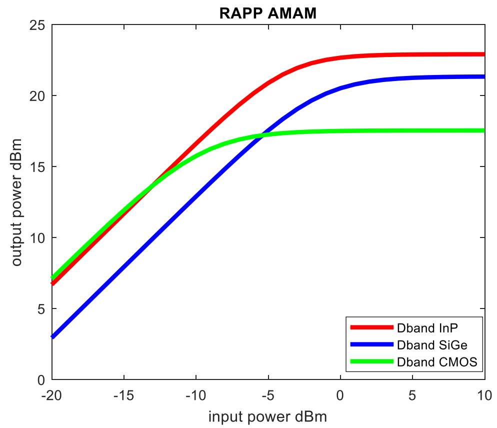


- Impact of Parallel-Hammerstein models with memory



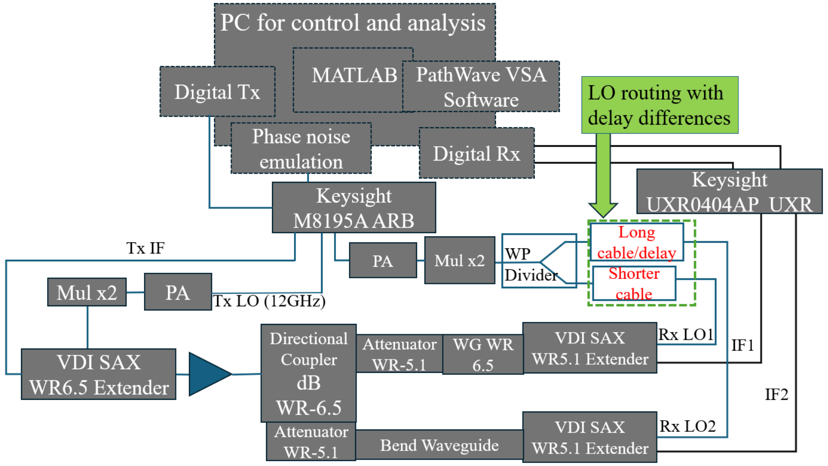
- AM/AM and AM/PM distortion for memoryless PAs

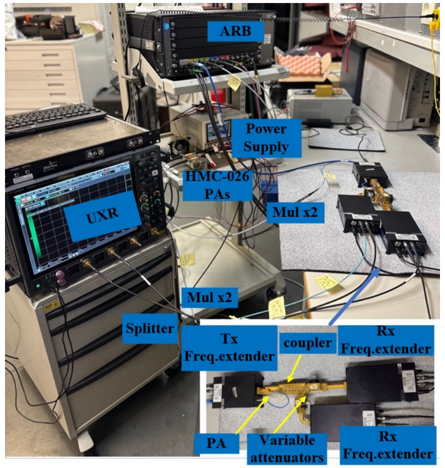




LO Delay-based Wideband Phase Noise (PN) Mitigation

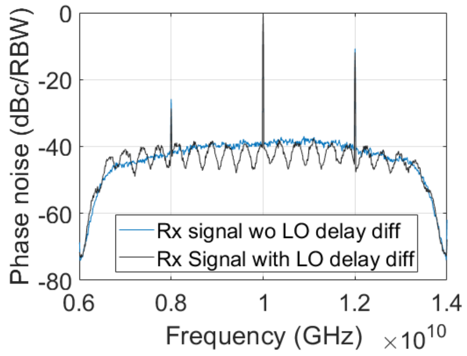
- PN reduction over multiple Rx paths with shared but delayed LOs was succesfully demonstrated with modulated signals at 150 GHz. Also, compensation strategies for arrays were studied. It was also observed that LO delay can help to reduce the impact of phase noise in monostatic sensing.

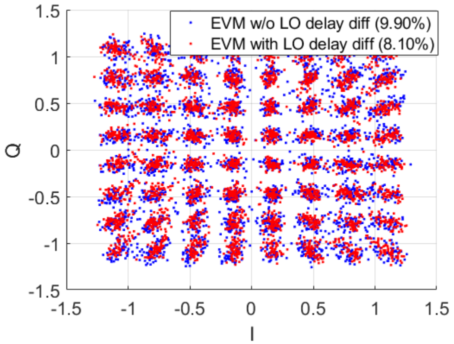




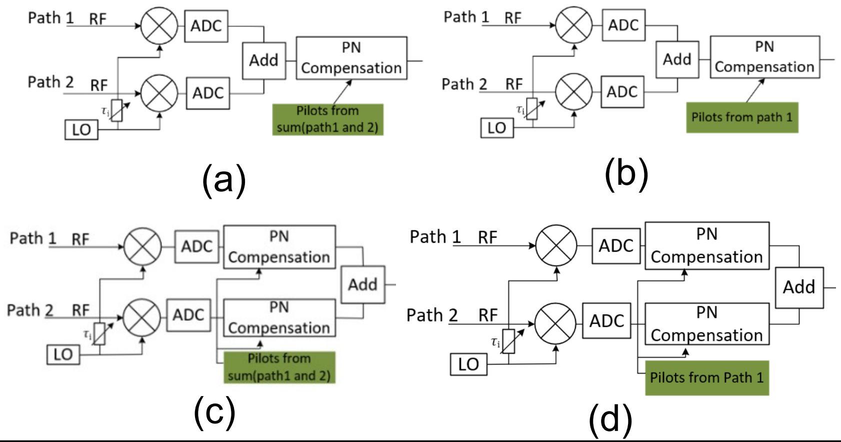
Tx noise floor $= -130\ dBc/Hz$

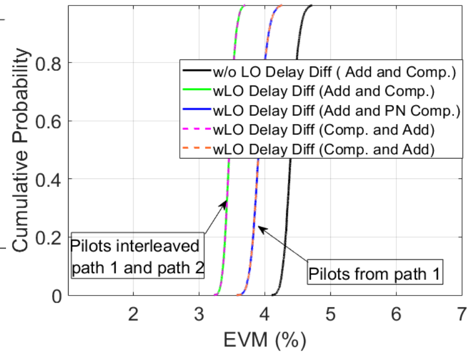
64-SC-QAM, B =1GHz



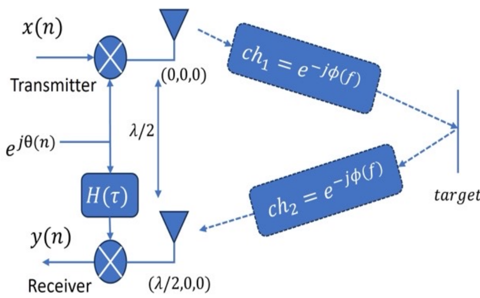


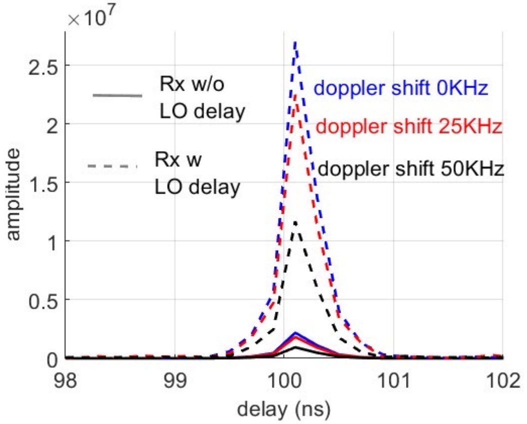
- PN compensation strategies with LO delay differences.





- Wideband PN reduction in monostatic sensing.





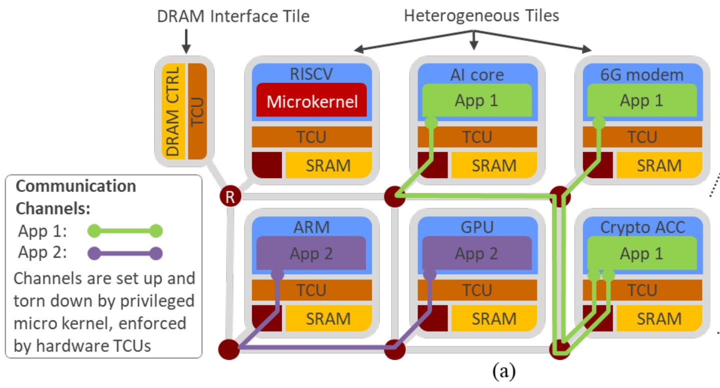
Reduced PN w delayed Rx LO

5. SoC Technologies

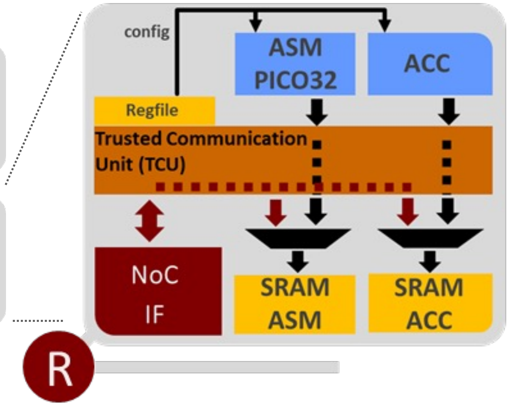
- Design of Secure and Scalable SoC Architecture
  - Integrated trustworthiness covering HW, runtime, and OS
  - Tiled computing architecture
  - Inter-tile communication channels fully controlled by micro-kernel OS and trusted communication units
  - Chip-prototype as proof of concept and performance and power consumption analysis
- HW Accelerators for Signal and AI Processing
  - Investigated signal processing requirements and estimated associated energy consumption
  - Developed SoC performance and energy consumption estimation methodology and application to software defined signal processing SoC
  - Design of AI accelerator architecture – chip prototype as proof of concept and performance and cost estimation

Secure SoC Architecture

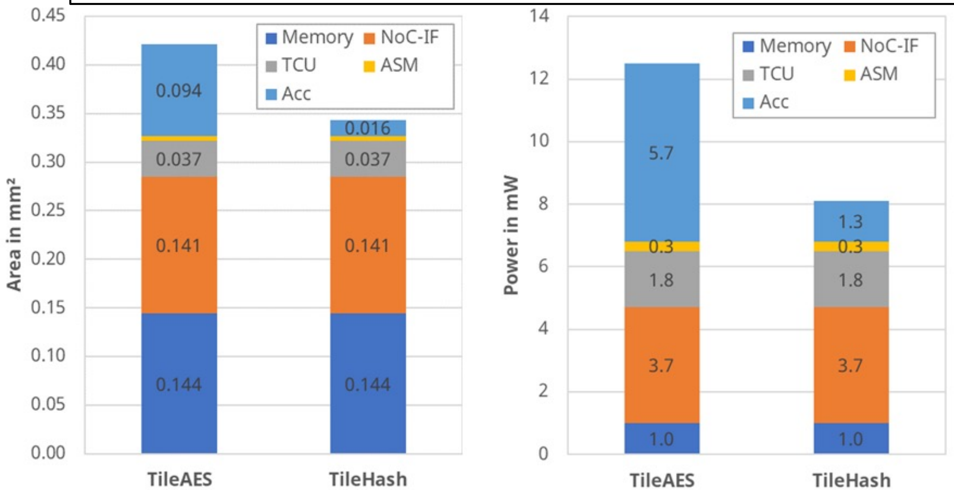
- Goal: Investigate secure connectivity of SoC HW/SW components by providing hardware-supported application isolation
- Challenge: Integration of non-programmable HW accelerators
  - Enable inter-tile communication and interface to operating system of a HW accelerator by introducing Accelerator Support Module (ASM)
  - Implemented SW multiplexer on ASM for scheduling and low-level memory management, allowing multiple applications to share the accelerator tile
  - Analyzed overhead: security-relevant parts consume about 11% area and 22% power



Accelerator (ACC) Tile with Accelerator Support Module (ASM)



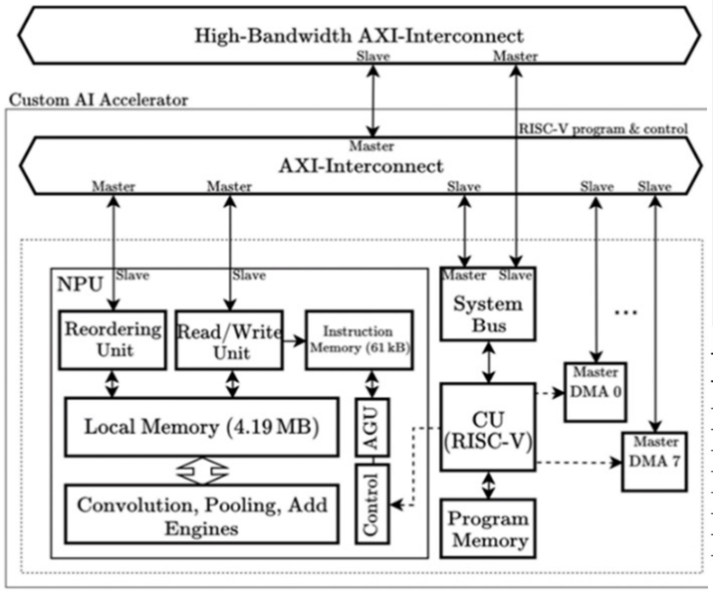
Security Overhead Analysis: Area (left) and power (right) consumption obtained from post-layout implementation of accelerator tiles. The ASM is the PicoRV32 RISC-V core.

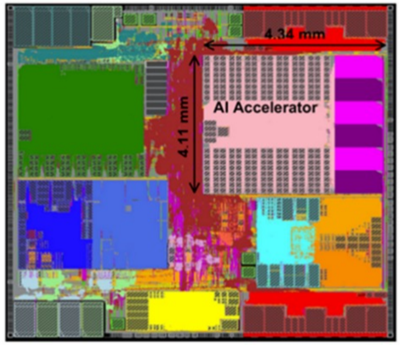


SoC AI and DSP Capability

- Goal:
  - Investigation of scalable SoC architectures for 6G baseband processing.
  - Focus on AI and DSP accelerators, accelerator design, analysis of performance and energy efficiency for specific use cases
- SoC and accelerator architecture exploration. Analysis of performance and power consumption requirements.

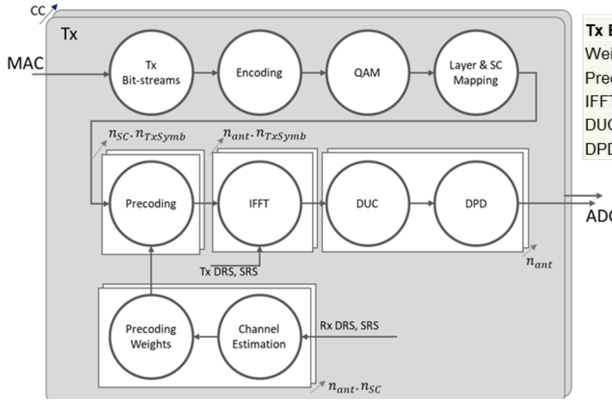
AI Accelerator Architecture



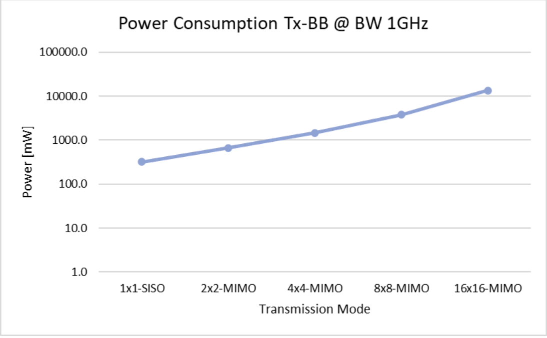


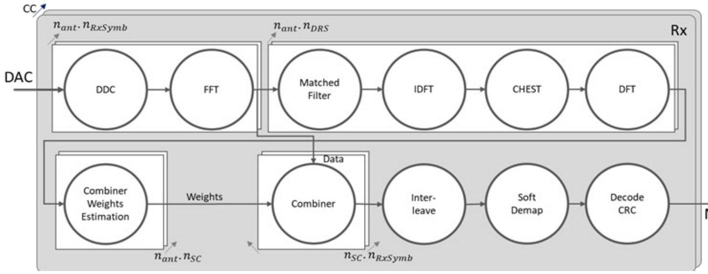
	SoC
Technology	GF 22 nm FDX
Area [mm²]	93.06
Logic Area [mm²]	65.14
Memory Area [mm²]	27.92
Core Voltage [V]	0.8
No. Transistors	1.8×10^9
On-Chip SRAM [Mbit]	91.25
Max. Supported Cameras	16
Max. Clock Frequency [GHz]	ARM A65AE: 1.2 ARM R52: 0.5 ISP: 0.6 AIA: 1.0

Acceleration of Tx-Rx Baseband Signal Processing

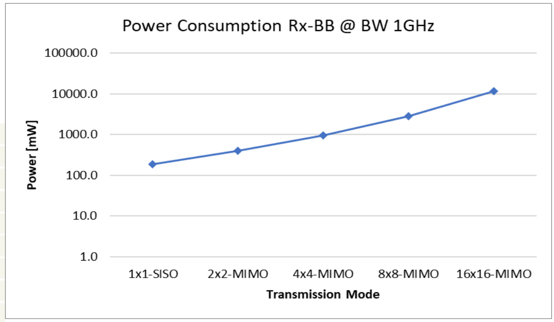


Tx Baseband Kernels
Weight estimation
Precoding
IFFT
DUC (Digital Up-Conversion
DPD (Digital Predistortion)





Rx Baseband Kernels
DDC (Digital Down-Conversion)
FFT
Matched Filter
IDFT
CHEST (Channel Estimation)
DFT
Weight estimation
Combiner



6. Ultra-low cost/power IoTDs & communication design

- Manufacturing, Deployment, and Energy Trade-offs
  - Materials and Manufacturing
  - ZED Design Study
  - AIoT deployment trade-off
- Energy, Cost, and Performance Trade-offs
  - Energy/cost analysis & future directions for eLPWA devices
  - Solar-powered ZED Prototypes
- Lightweight and Energy-Aware Protocols
  - Lightweight Protocols
  - Energy-aware Protocols
- Multi-source EH and Intelligence
  - Multi-Source EH
  - Tiny ML and Distributed Intelligence
- Duty-cycling, Wake-up, and RF-WPT
  - Duty-cycling and Wake-up Protocols
  - RF-WPT

Manufacturing, Deployment, and Energy Trade-offs

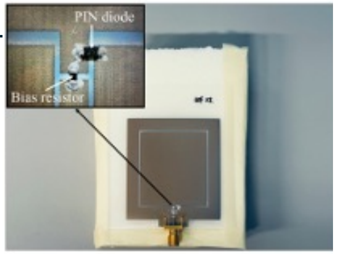
➢ Materials and Manufacturing

Material selection based on the device design and process
- Inks
- Conducting materials
- Semiconducting materials
- Dielectric materials
- Substrates
- Synthetic polymers
- Natural polymers

Printing process
- Contact printing
- Non-contact printing

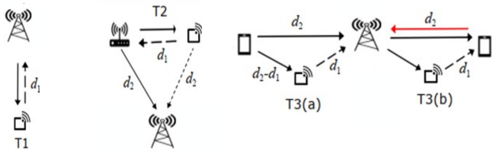
Post-printing process
- Thermal sintering
- Photonic sintering
- Plasma sintering
- Microwave sintering
- Electrical sintering
- Chemical sintering

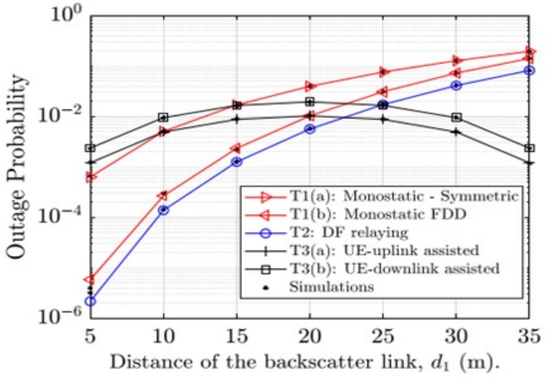
Manufacturing process for printed electronics

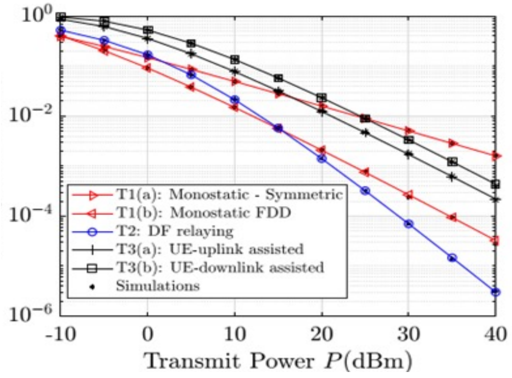


Printed backscatter antenna with surface-mounted PIN diode switching element

➢ AIoT deployment trade-offs

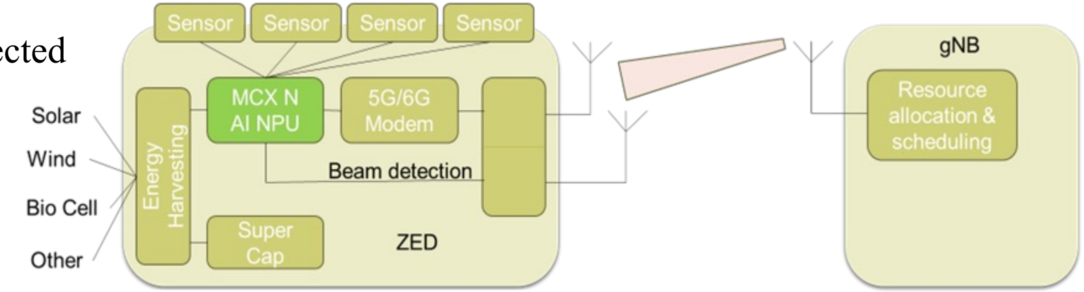


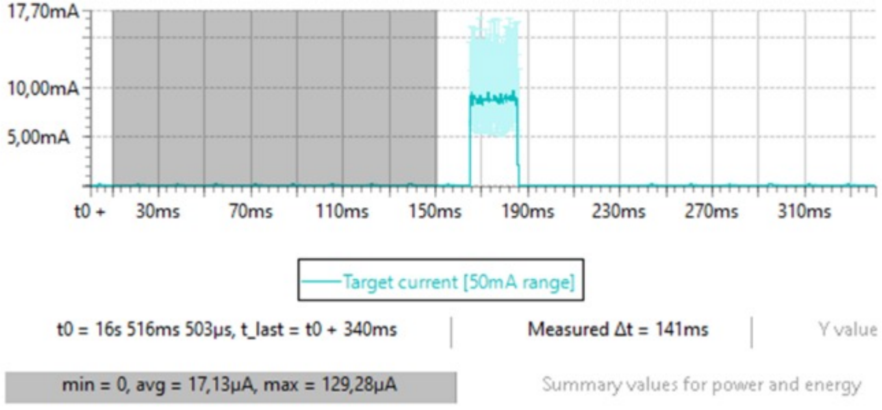




➢ ZED Design Study

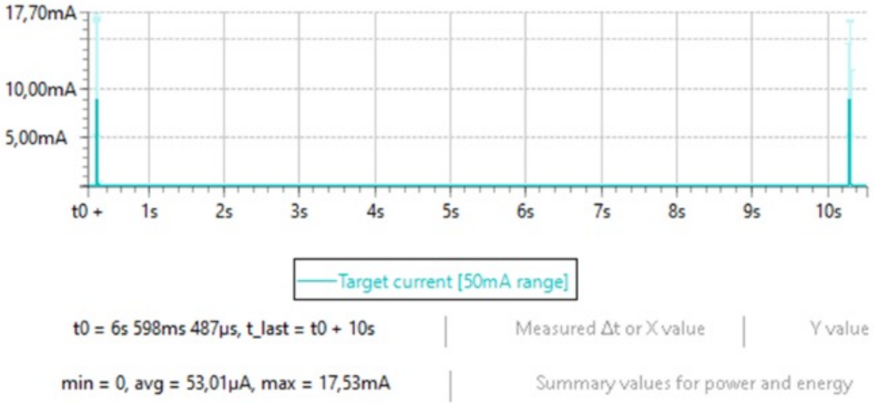
ZED connected to a gNB





Average current consumption during power down

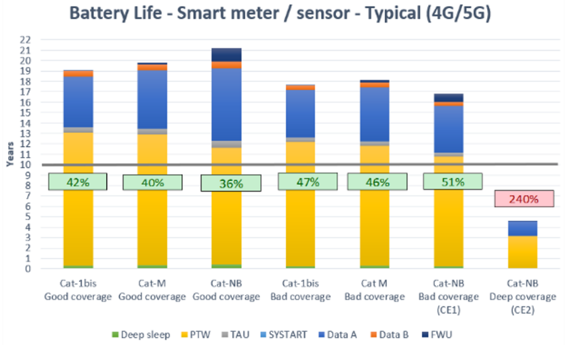
Average current consumption for a sensor reading interval

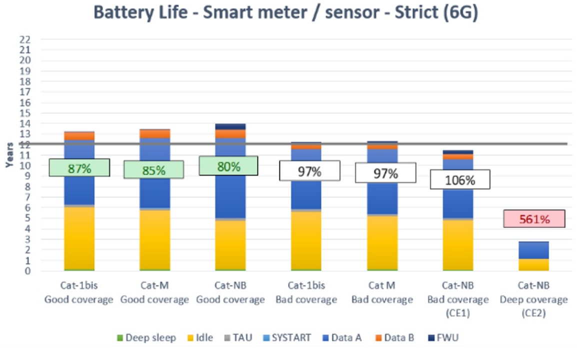


Energy, Cost, and Performance Trade-offs

➢ Energy/cost analysis & future directions for eLPWA devices

Battery lifetime comparison of legacy IoTDs for typical (4G/5G-like) & strict (6G-like) applications

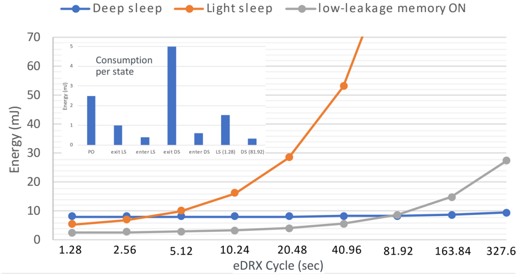




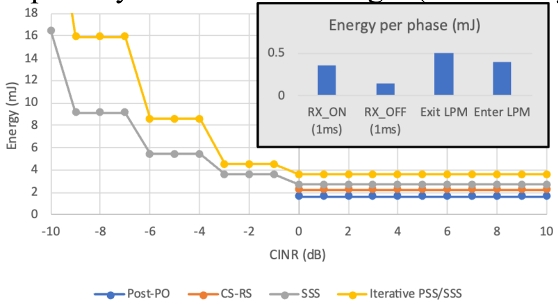
Cost comparison of 4G/5G cellular IoTDs

Cost Component	Cat-NB1 (HD-FDD)	Cat-M1 (HD-FDD)	Cat-1bis (FD-FDD)	eRedCap (FD-FDD)
Die (RF/Analog)	– 60%	– 50%	10%	+ 20%
Die (BB/Digital)	– 70%	– 40%	20%	+ 30%
Die (PMU*)	– 40%	– 30%	5%	+0%
Die (Peripherals, other)	– 30%	– 30%	7%	+20%
Memory (Flash, RAM)	– 50%	– 30%	8%	+50%
PA	– 50%	– 30%	8%	+ 50%
LNA	– 100%	– 100%	2%	+0%
Mechanics (PCB, shield)	– 40%	– 20%	6%	+0%
Clocks	– 20%	– 20%	4%	+0%
RF switches	– 50%	– 50%	6%	+0%
Duplexers	– 100%	– 100%	19%	+0%
Other (passives)	– 45%	– 45%	5%	+10%
Total	**~40%**	**~50%**	**100%(Ref)**	**~120 %**

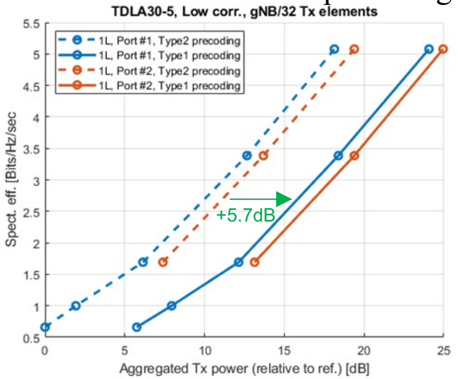
Optimised sleep strategy (eDRX cycle example)



Adaptive synchronization design (PO activity example)

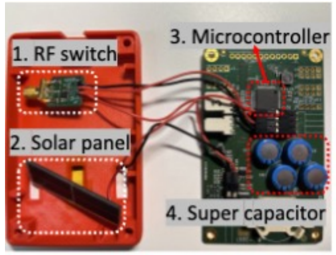


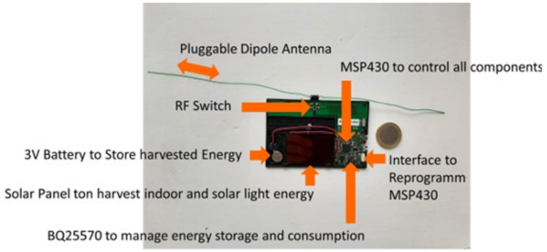
1Rx devices with advanced precoding at BS



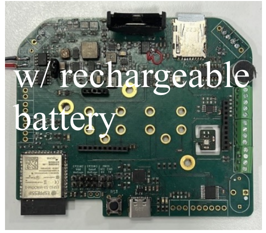
➢ Solar-powered ZED Prototypes

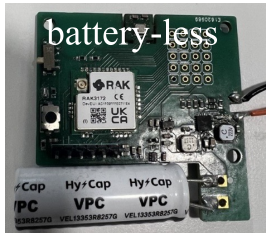
Backscattering ZED





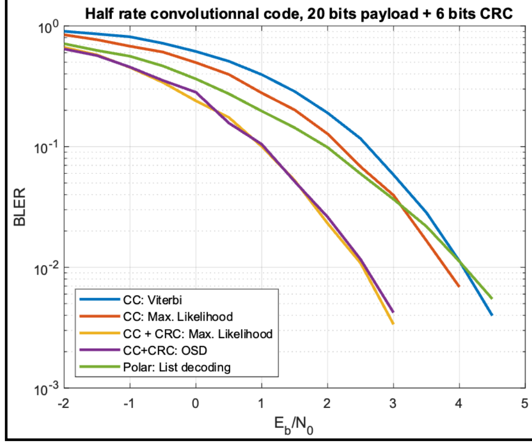
Active ZED



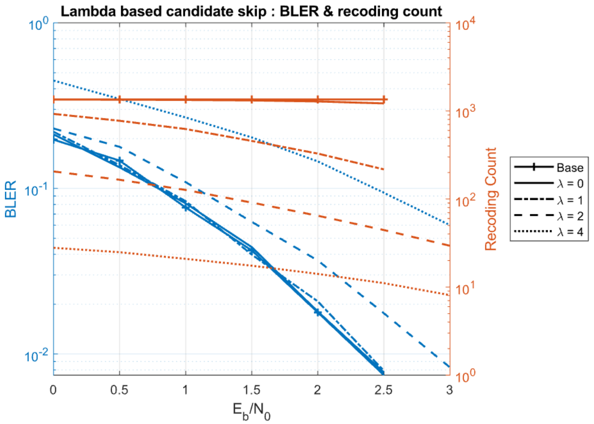


➢ Channel Coding

Joint decoding CC+CRC with OSD



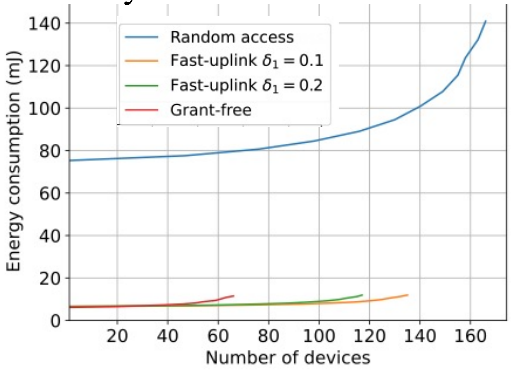
Optimization: skip codeword depending on parameter λ



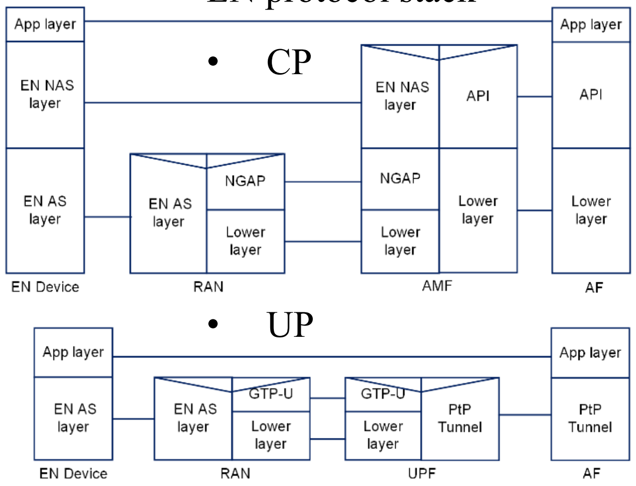
Lightweight and Energy-aware Protocols

➢ Lightweight Protocols

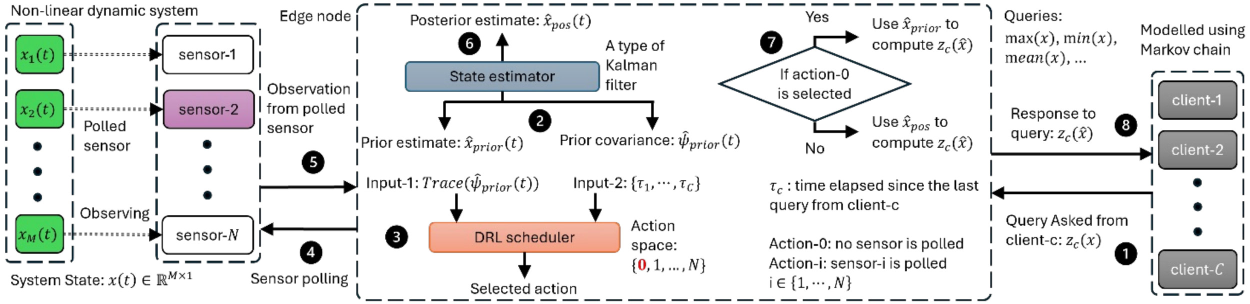
Fast-uplink evinces better energy efficiency trade-offs



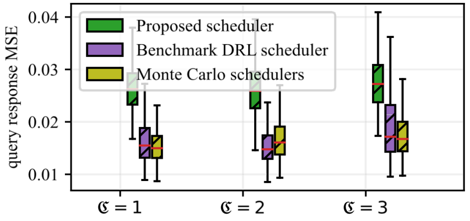
EN protocol stack

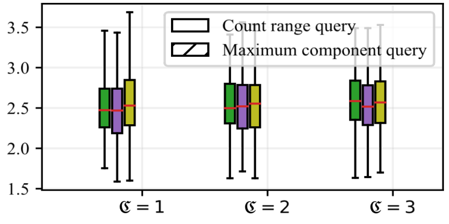


Goal-oriented sensor reporting scheduling to reduce signal overhead



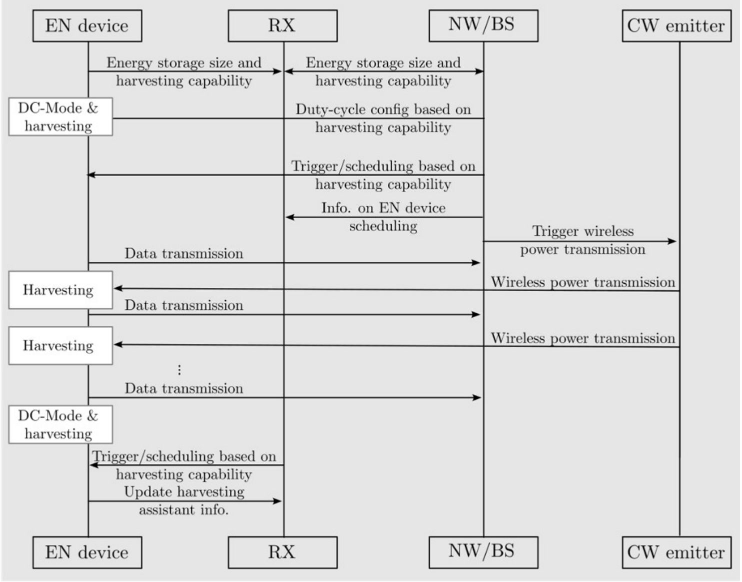
- two clients
- C: combinations of different client types

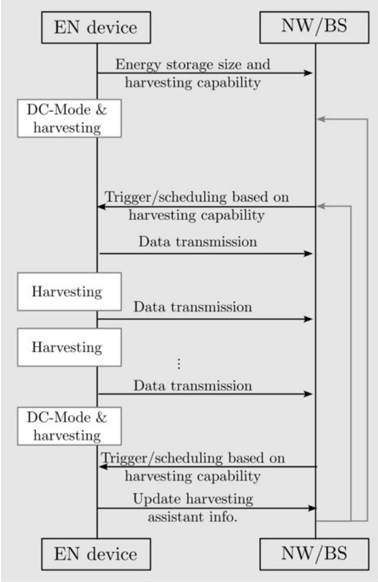




➢ Energy-aware Protocols

Adaptive UL transmission and DL monitoring/reception



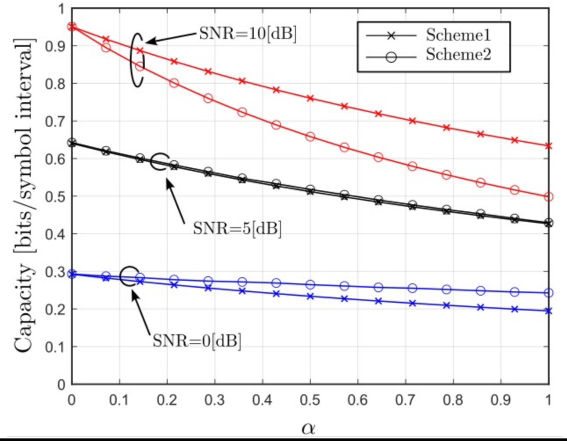


network/BS & Rx are: separate entities or the same entity

Adaptive backscattering

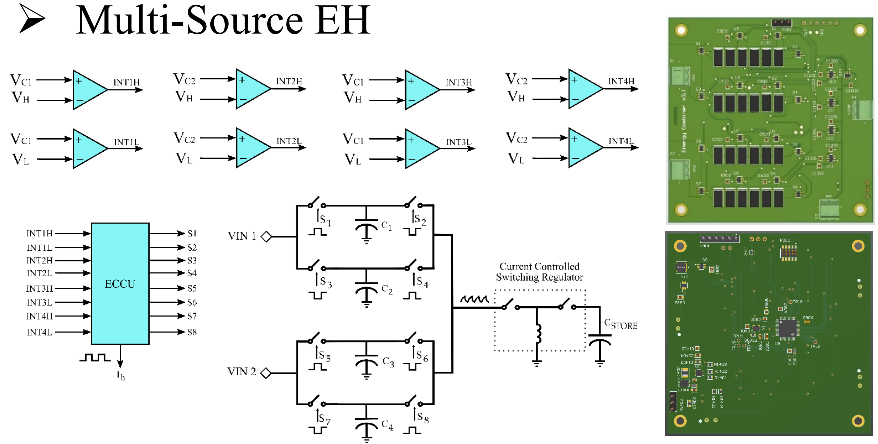
To boost the harvested energy:

- Scheme 1: adding (dummy) 0s to allow for RF-EH
- Scheme 2: extending the symbol period



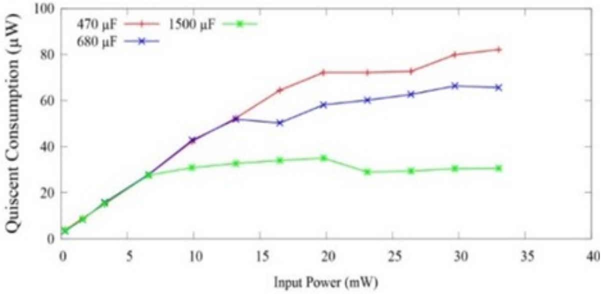
Multi-source EN and Intelligence

➢ Multi-Source EH



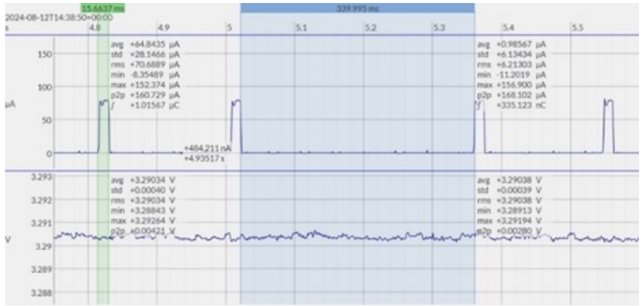
High-level schematic and 3D render of the PCB of the EC

Average power consumption of the circuit



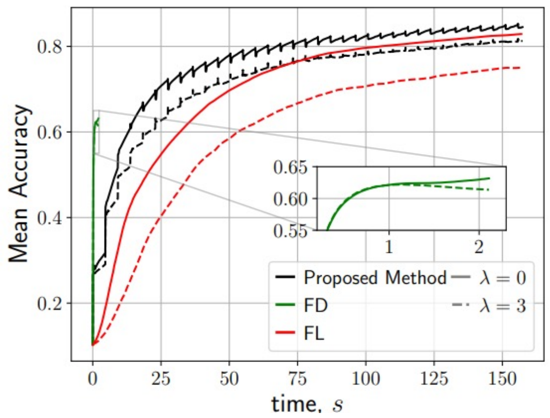
with respect to input power for different temporary buffer values

power profile of the intermittent wake-ups

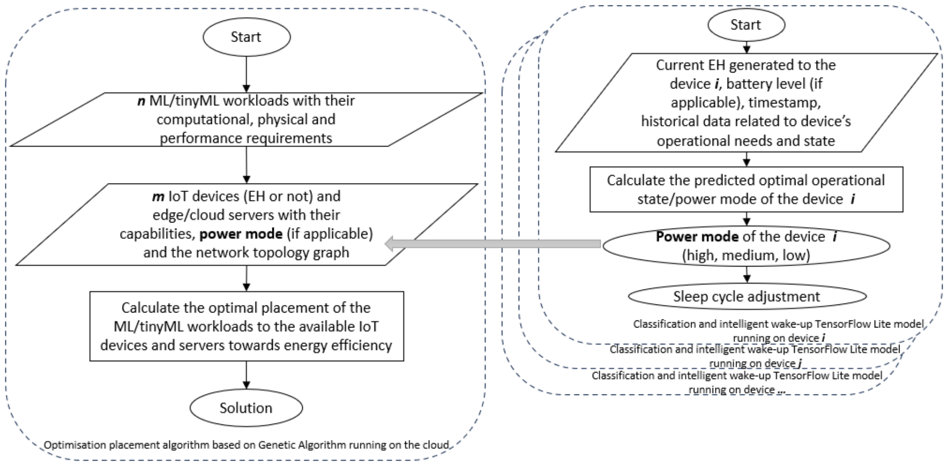


➢ Tiny ML and Distributed Intelligence

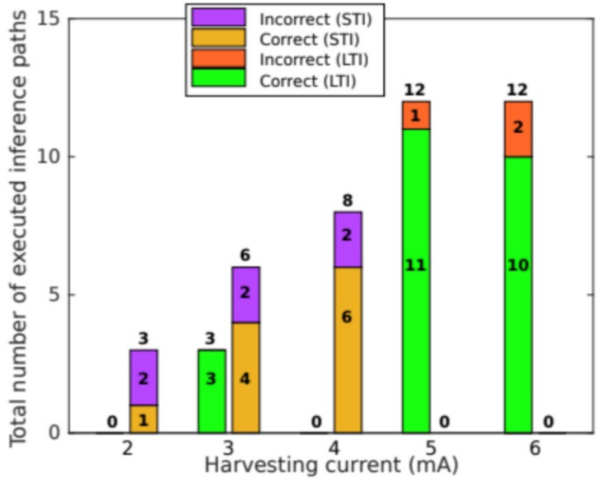
Federated learning with distillation switch

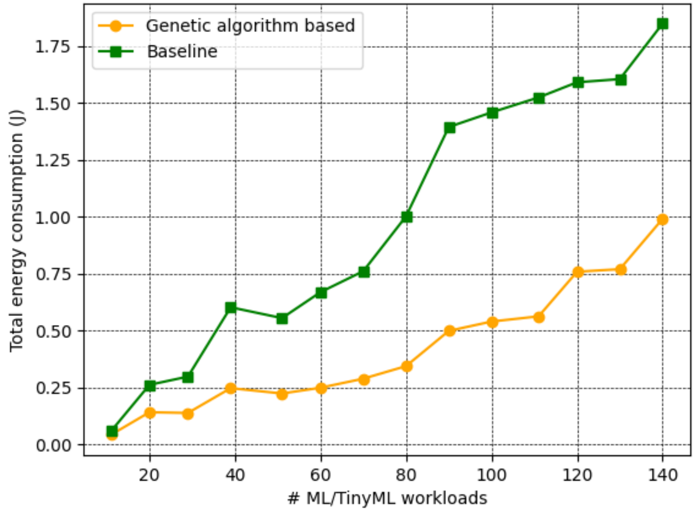


Distributed intelligence for ML/TinyML workload's placement



Energy-aware tinyML model selection



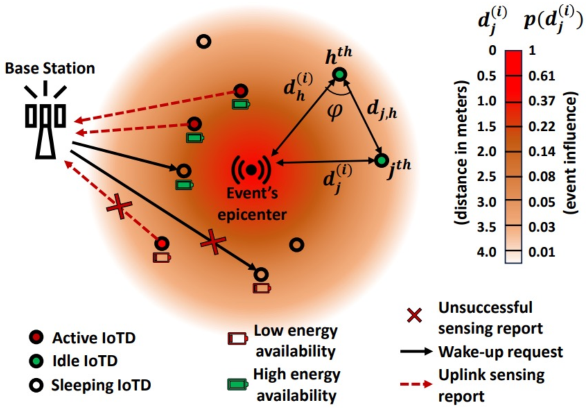


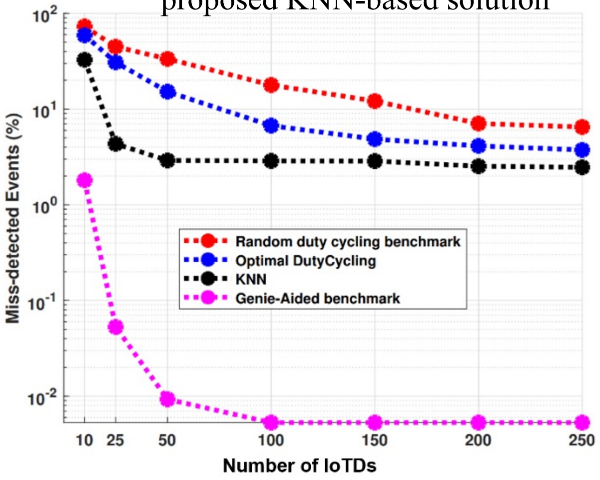
Duty-cycling, Wake-up, and RF-WPT

Duty-cycling and Wake-up Protocols

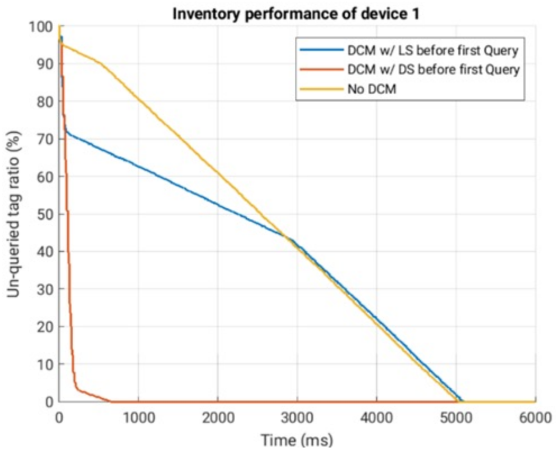
Intelligent duty-cycling and wake-up exploiting spatial correlations for an IIoT alarm scenario

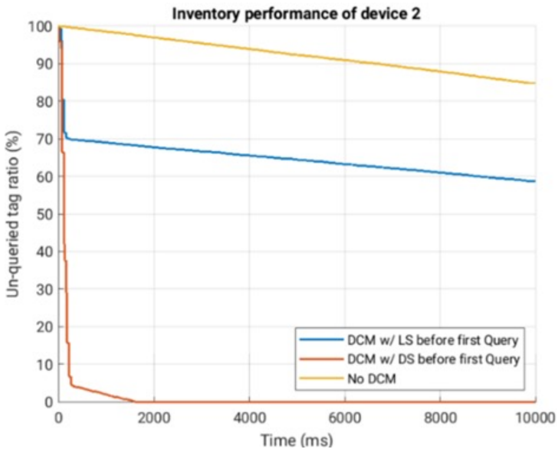
proposed KNN-based solution





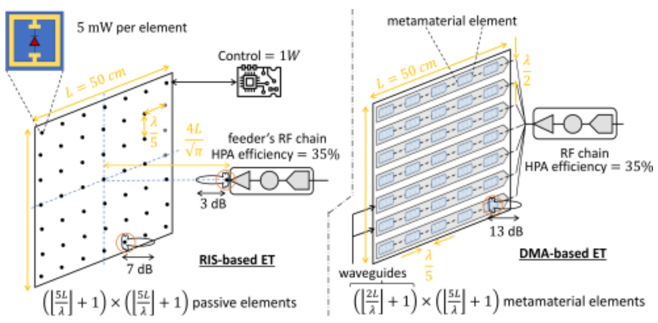
Duty-cycle monitoring for inventory/command

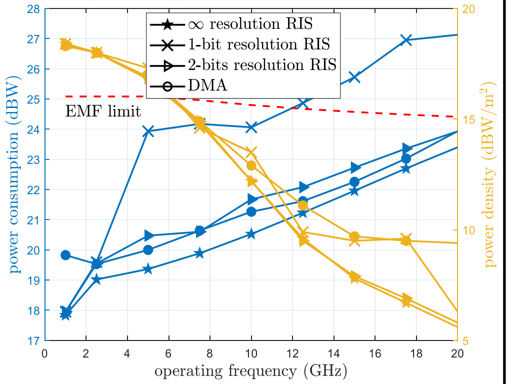


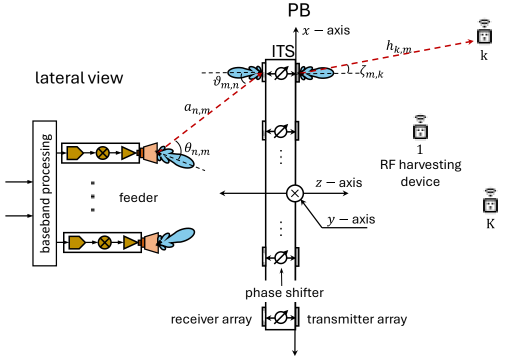


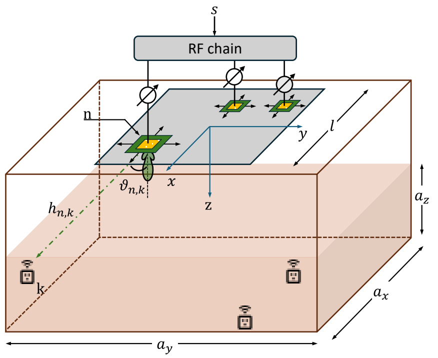
RF-WPT

Energy-efficient and scalable PB Transmit Architectures

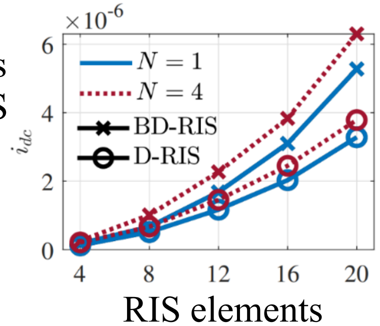


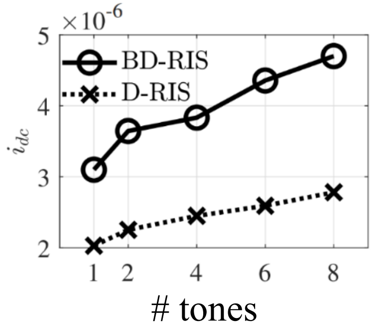






Diagonal (D) RIS vs Beyond-D (BD) RIS for WPT

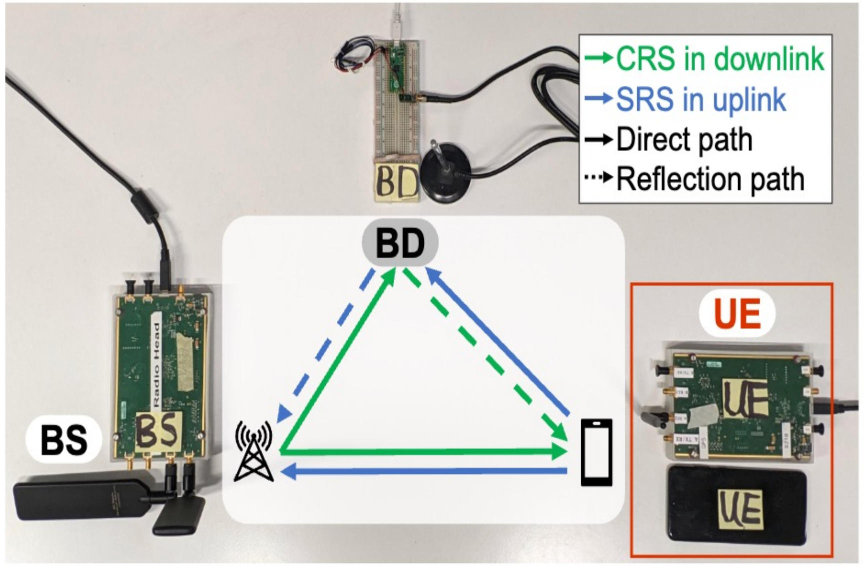


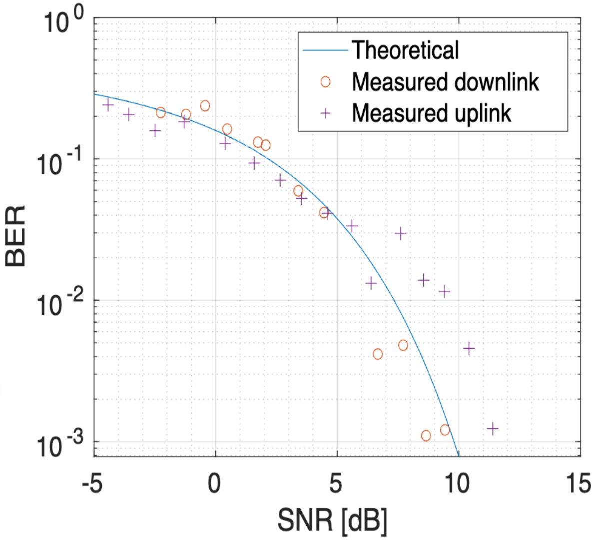


7. PoCs

- Cellular-backscattered ZEDs
- Scalable E2E XR Testbed

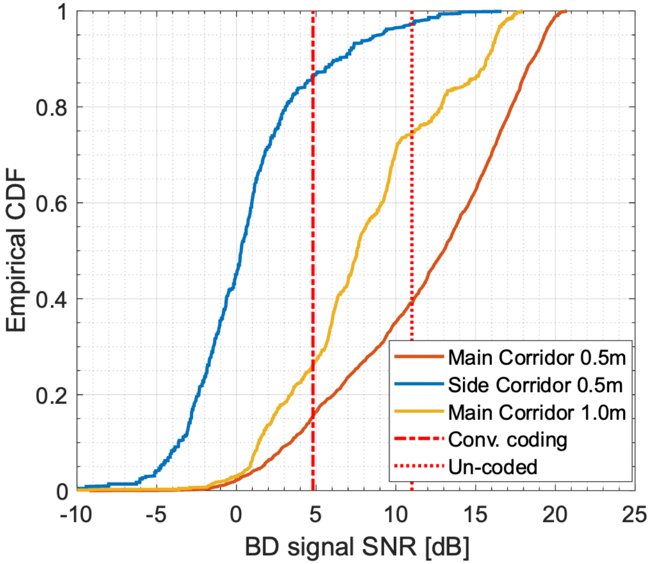
Cellular-backscattered ZEDs





Improving BD channel reliablity by using convolutional codes and CRC.

Field trial using commercial LTE network and SDR implementation of UE



Uplink: User Equipment (UE) transmits Sounding Reference Signals (SRS) that illuminate the Backscatter Device (BD). The Base Station (BS/eNodeB) receives the SRS, estimates the channel, and demodulates the BD message.

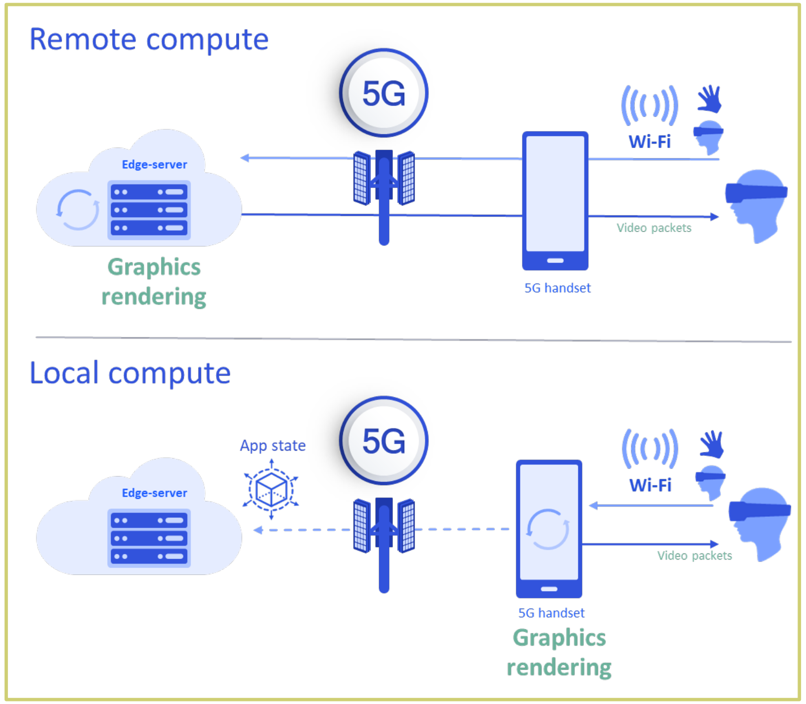
- Transmitter: Commercial mobile phone
- Receiver: Software defined radio (SDR) implementation of eNodeB.

Downlink: The BS transmits Cell-Specific Reference Signals that illuminate the BD. The UE estimates the channel and demodulates the BD message.
SDR implementation of UE was used to implement BD receiver.

- Transmitter: SDR implementation of eNodeB
- Receiver: SDR implementation of UE

E2E Scalable XR

- Goal: to demonstrate the benefits of Scalable Compute, where a) intensive processing tasks are offloaded to a dedicated remote server instead of the local device, and b) the application bit rate is adjusted to meet the requirements in terms of throughput and latency.
- Challenge: the proposed solution requires a tight coordination between the applications, infrastructure and devices. These elements form a foundation for 6G networks, incorporating features such as low latency, low loss Scalable throughput (L4S) and adaptive rate control (ARC) APIs.
- Results showing L4S's benefits for adaptive rate control, enhancing user experience, latency and quality, will be included in D2.6.



Scalable XR with dynamic spatial compute
- (top) In good radio and network the compute can be done remotely, to save power in the headset
- (bottom) If conditions are not good enough, the processing is done locally

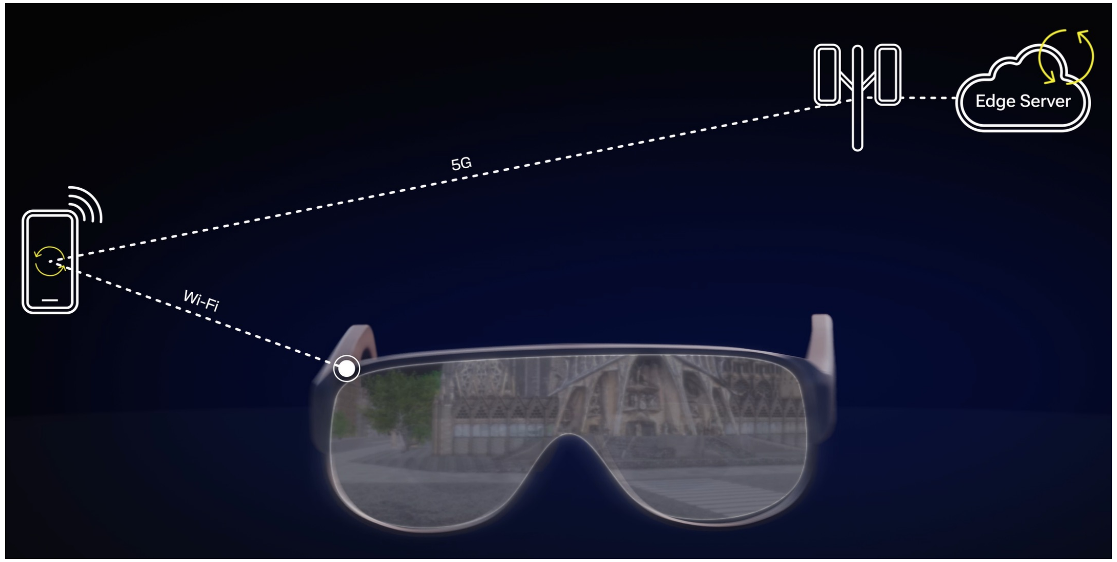


Illustration of the testbed setup: with the AR glasses running the client application, the companion device with a 5G connection to the Network and the rendering server for the remote computing.

6. Conclusions

- Refinement of 6G device classes, linking updated use-case requirements to technology enablers.

  Four novel 6G device classes were analysed and their KPIs quantified, while sensing was explored as a feature for some, laying the groundwork for addressing diverse 6G service needs.

- Notable advancements in FR1, FR2, FR3, and sub-THz transceivers, including new emerging and promising technologies like RTDs and RIS.

- Developments in SoC architectures, including secure, energy-efficient designs and scalable HW solutions for signal processing and AI acceleration.

  A ”trusted SoC” and AI accelerator architecture with mixed precision arithmetic was provided.

- Energy/cost assessment of IoTDs and novel approaches to ultra-low-cost/power designs.

  Two ZEDs were proposed, built, and tested under both laboratory and field conditions. Several technology enablers were studied and developed further. Various UL access mechanisms for cellular IoT networks were assessed. Low-complexity/power multi/fluid transmit antenna architectures were conceptually evaluated for RF-WPT purposes.

- Two PoCs were presented while validating the practicality of key innovations.

  They showcased how zero-energy IoTDs and scalable XR E2E solutions can be deployed in real-world scenarios

An extensive exploration of techn. advancements, designs, and validations essential for 6G devices and infrastructure!!

HEXA-X-II

HEXA-X-II.EU //

Co-funded by the European Union

6GSNS

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