High-Efficiency Power Amplifiers and Transceivers Leveraging Heterogeneous Integration Technologies

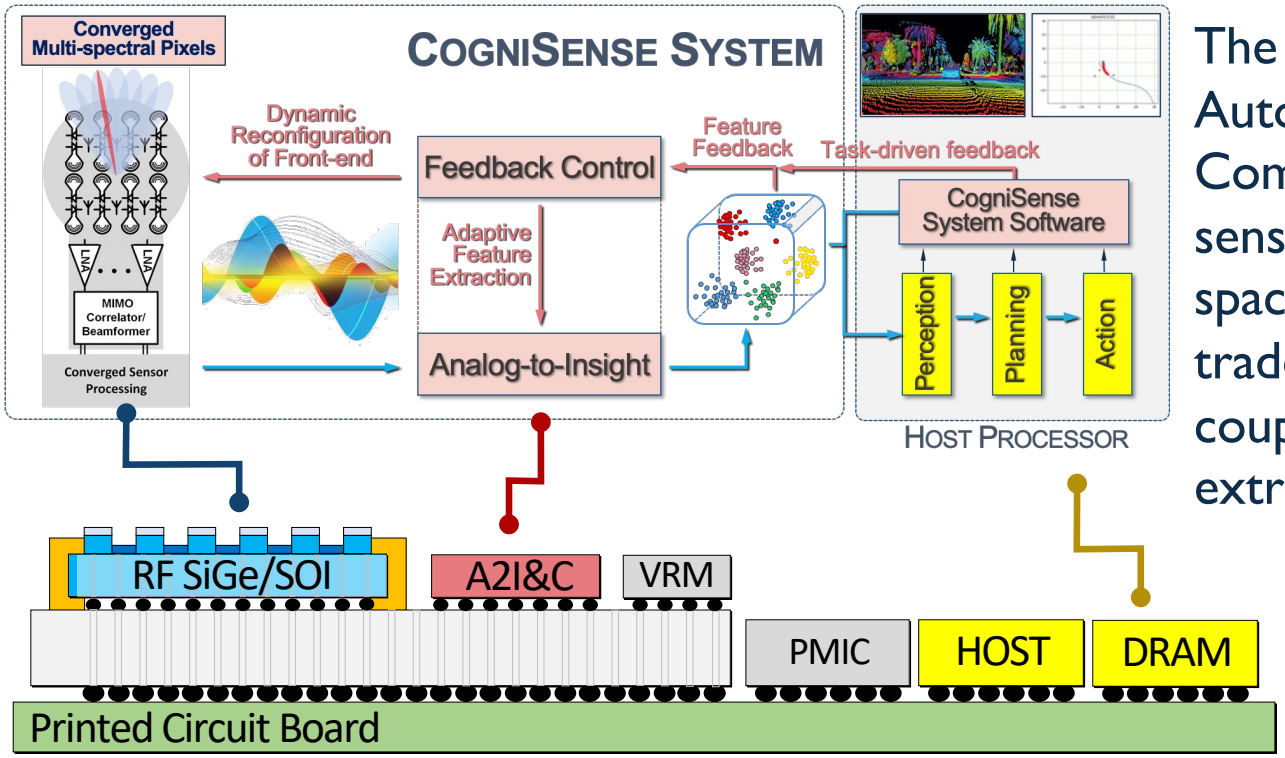
PI: Jim Buckwalter

UCSB
UNIVERSITY OF CALIFORNIA
SANTA BARBARA

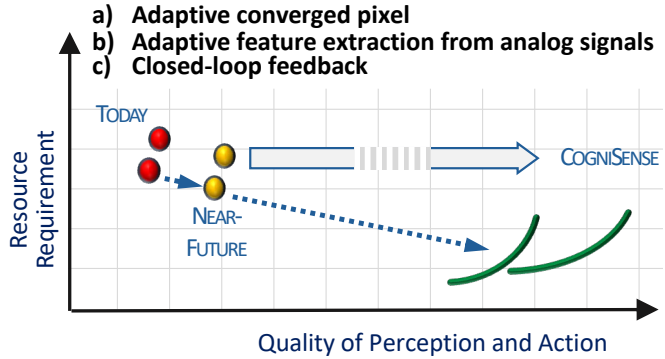
PseudolithIC

European 6G Flagship Hexa-X-II

6G: Fusing Communications and Sensing



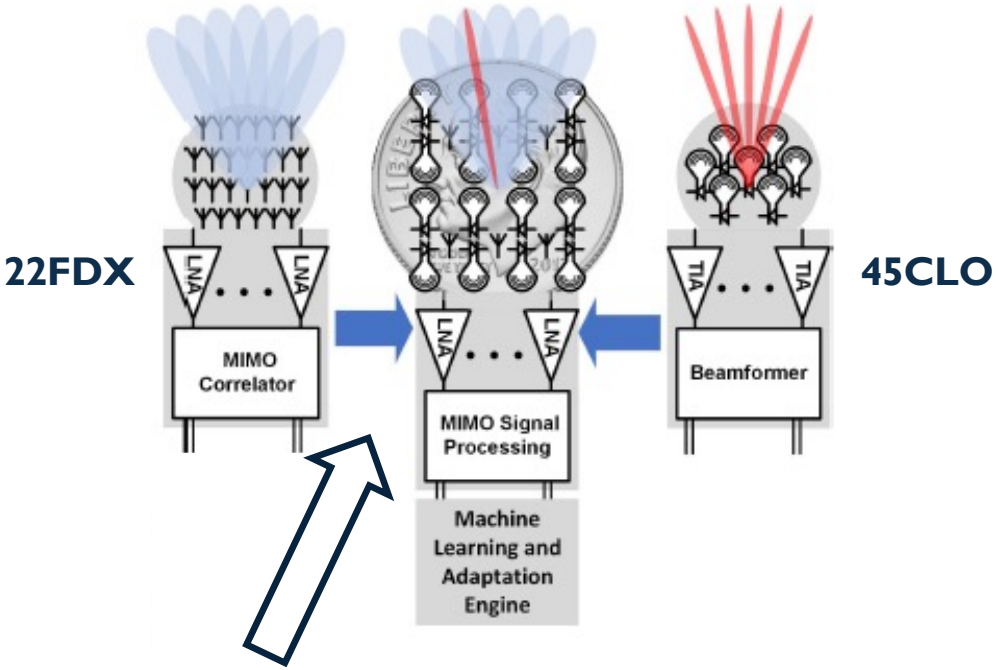
The Eyes, Ears, and Nervous System of Autonomous Systems:
Communication circuits will merge with sensors that explore the quality-resource space to dynamically traverse this tradeoff using closed-loop attention coupled with adaptive sensing and feature extraction.



Integration of Sensors Front-ends on CMOS

Objective: Advancing the capability of mm-wave MIMO radar and lidar to achieve sensor convergence with communications and adaptation for energy-efficient feature detection.

- Produce a rich set of sensing data by simultaneously combining
  - Millimeter-wave radar
  - Lidar
- Leverage low-power MIMO signal processing for communication and sensing
- Adapt front-end circuitry through machine learning engine

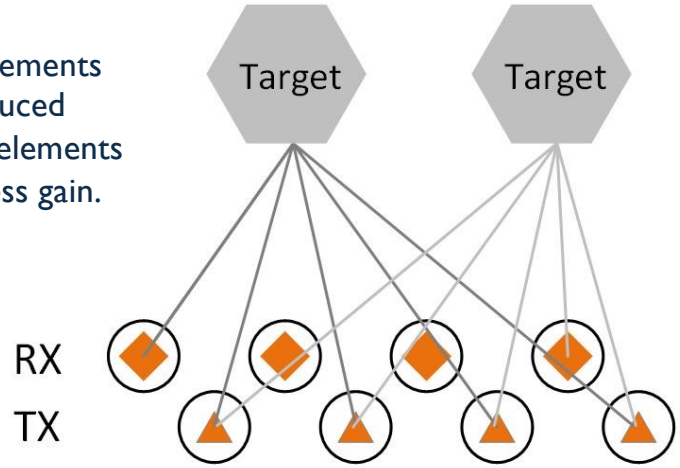


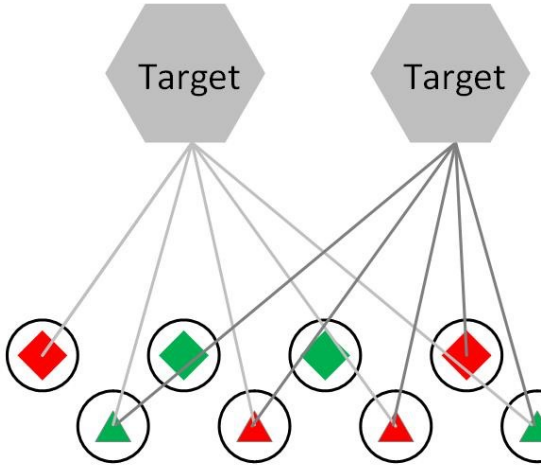
What are the technology solutions to integrate D-band radar and lidar?

Power Consumption in MIMO Radar

- Radar sensing energy depends strongly on the near-far problem
- Near objects with large cross section should require low PDC.
- How much power is required to detect multiple objects?

Case 1: All TX elements transmit the reduced power (and RX elements operated with less gain.





Case 2: Some TX and RX elements turn off to save power

$$P_{DC,RX} = P_{DC,0} + \frac{P_{DC,1}}{(F-1)}$$

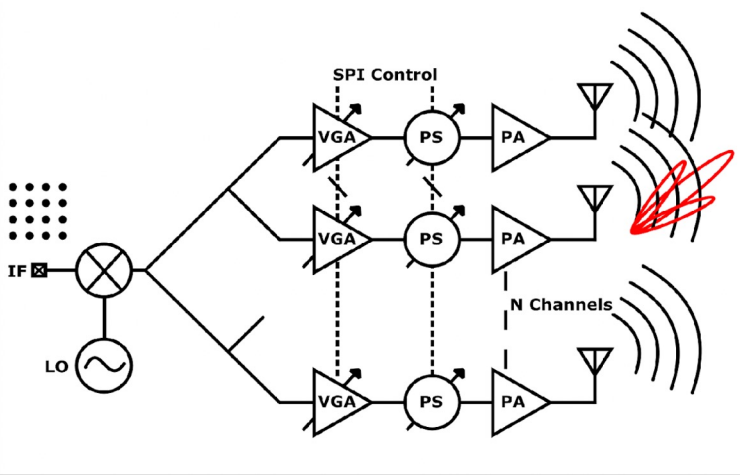
$$P_{TX} = R^4 \frac{SNR_{MIN}(4\pi)^3 k T_S B_n}{G^2 \lambda^2 \sigma}$$

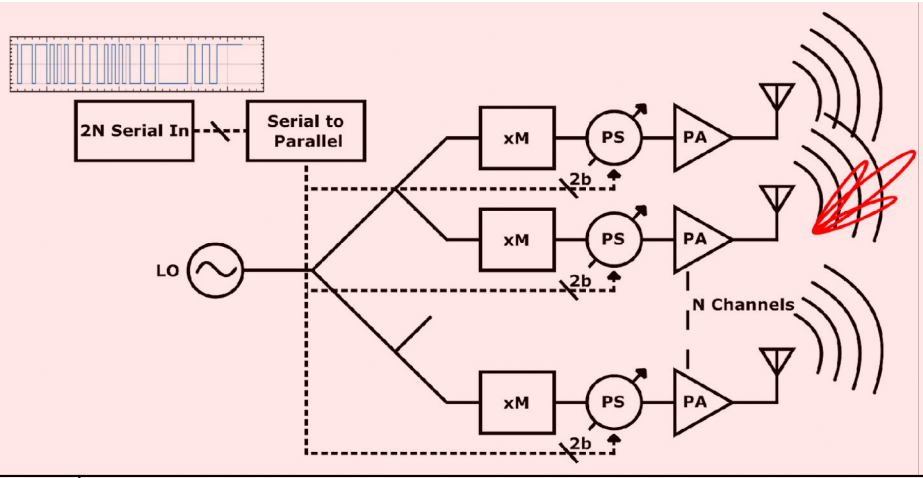
$$P_{DC} = N_{TX} P_{DC,TX} + N_{RX} P_{DC,RX}$$

$$P_{DC,OPT} = N_{TX} \frac{P_{TX} F_{OPT}}{\eta_{TX}} + 2\sqrt{N_{RX}} \frac{P_{DC,1}}{F_{OPT}-1} + N_{RX} P_{DC,0}$$

Higher frequency (lower λ) always requires a power penalty

Efficient Joint Communications and Sensing Transmitter

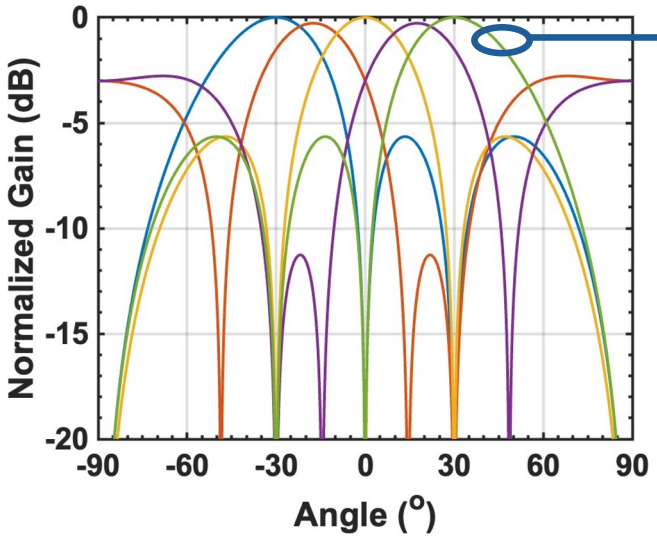




	Traditional RF Beamforming Array	Proposed Low-Resolution Digital Beamforming Array
Pros	• Uniform control • Linear transmit chain • Good sidelobe suppression	• Avoid linear PAs / always operate at peak efficiency • Slow/fast phase control switches between BF and MIMO • Supports SC/FMCW/OFDM
Cons	• Requires linear PA and/or backoff operation • Slow phase control • Less efficient	• Quantized control • Slightly lower array factor • Worse sidelobe suppression for small arrays

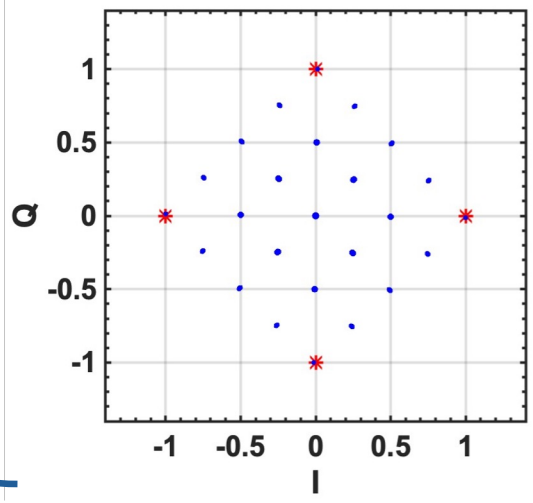
Architecture Supports Sensing and Communication

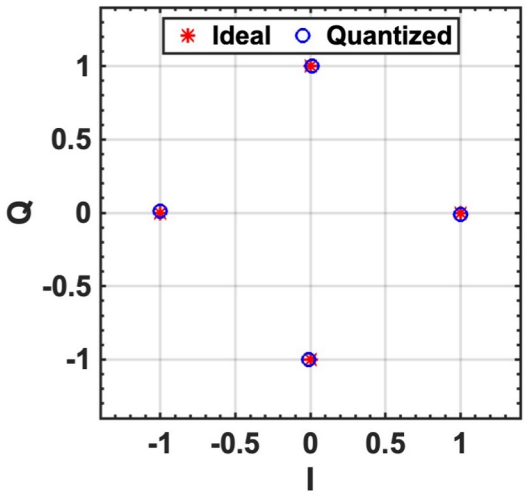
- 4-channel array simulation
- QPSK Modulation
- Direction: -30° to 30° in 15° steps.



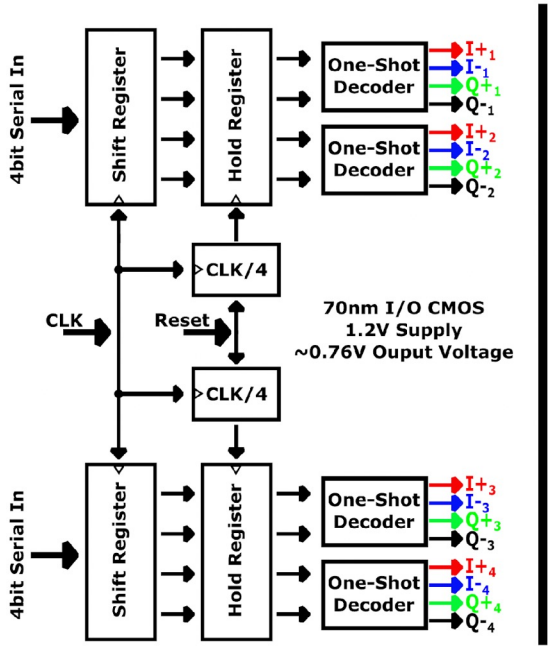
Unique constellation and phase settings for each beam

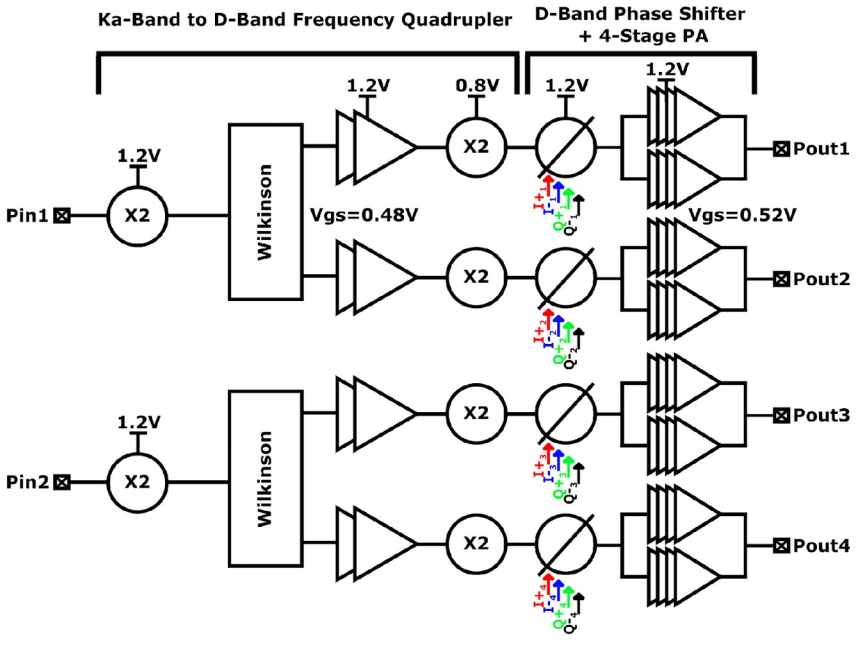
	Ch. 1	Ch. 2	Ch. 3	Ch. 4
00	0	90	180	270
01	90	180	270	0
10	180	270	0	90
11	270	0	90	180

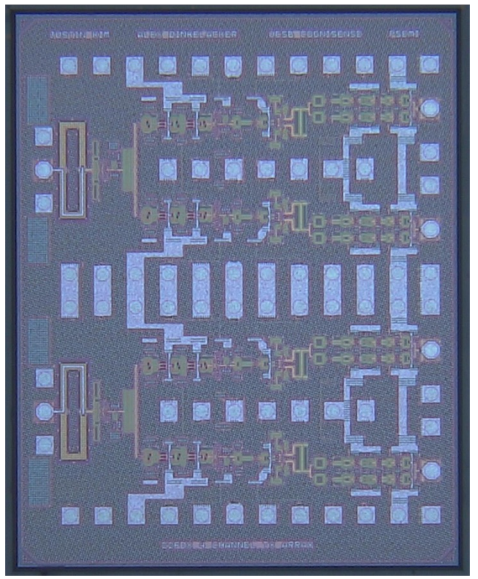




Full 4-Channel TX Architecture



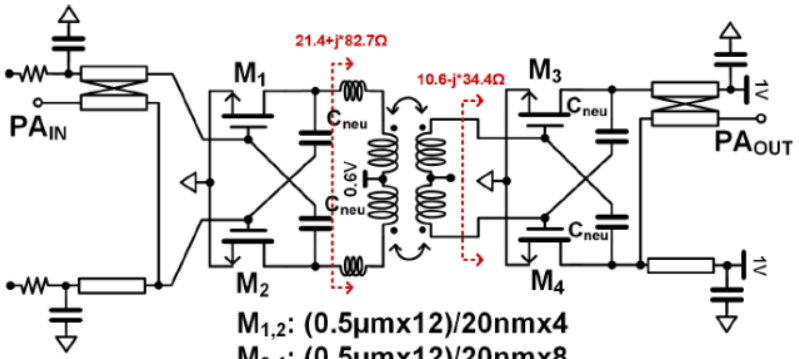


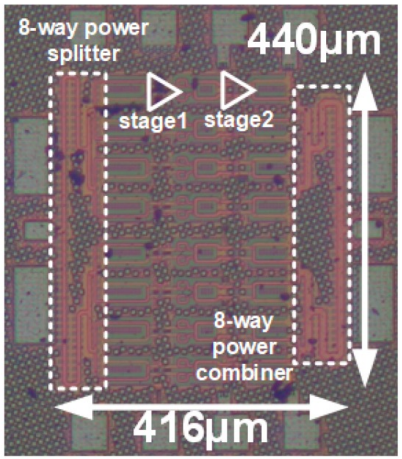


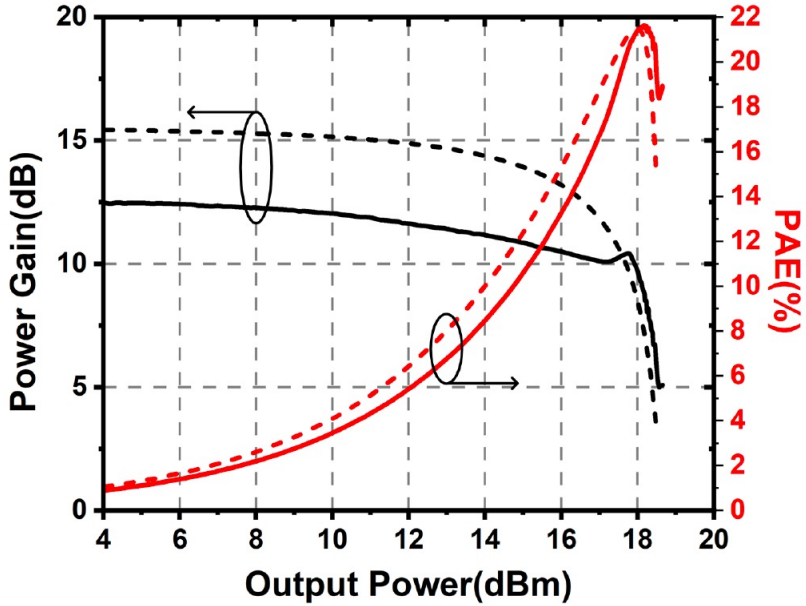
- 2 serial links provide I/Q control across the 4 channels.
- The serial data is demultiplexed into a pair of 4 one-hot phase control signals.
- Digital circuits based on TSPC logic that operate to 20 GHz (in 22FDX)

PA Measurements at 110-140 GHz using 22FDX

- Record PAE in a Silicon/Silicon-Germanium process in D-Band
- 22FDX offers significant promise for highly integrated modules.



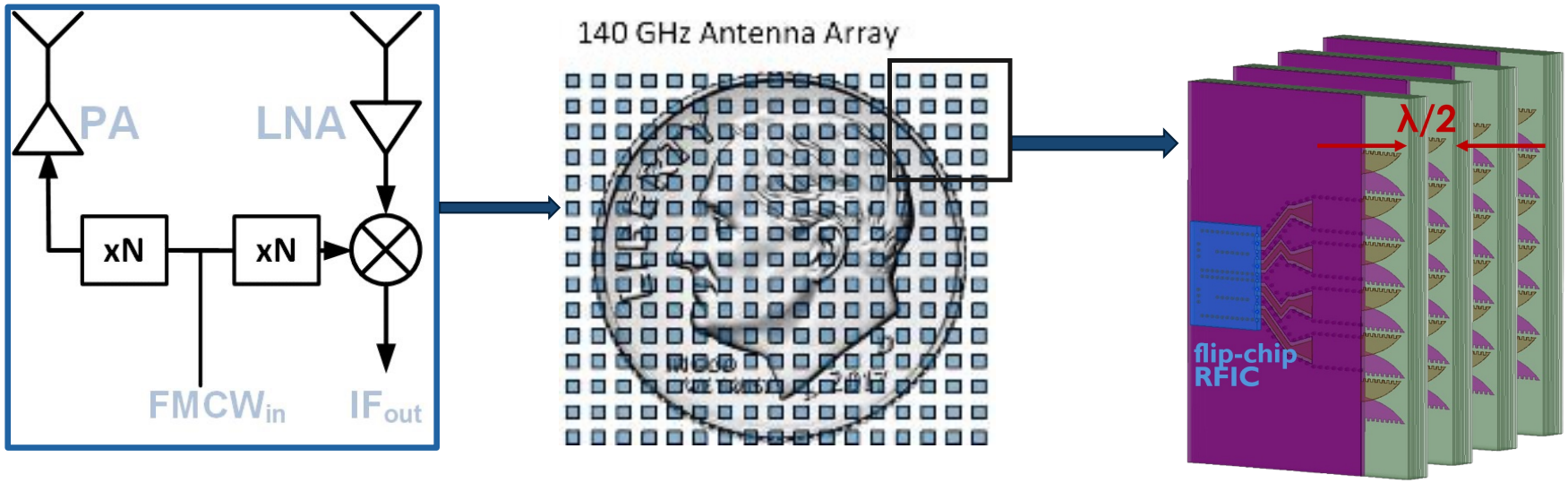




Ref: J. Shien et al., "An 18.6-dBm, 8-way-combined D-band Power Amplifier with 21.6% PAE in 22-nm FD-SOI-CMOS," BCICTS 2023

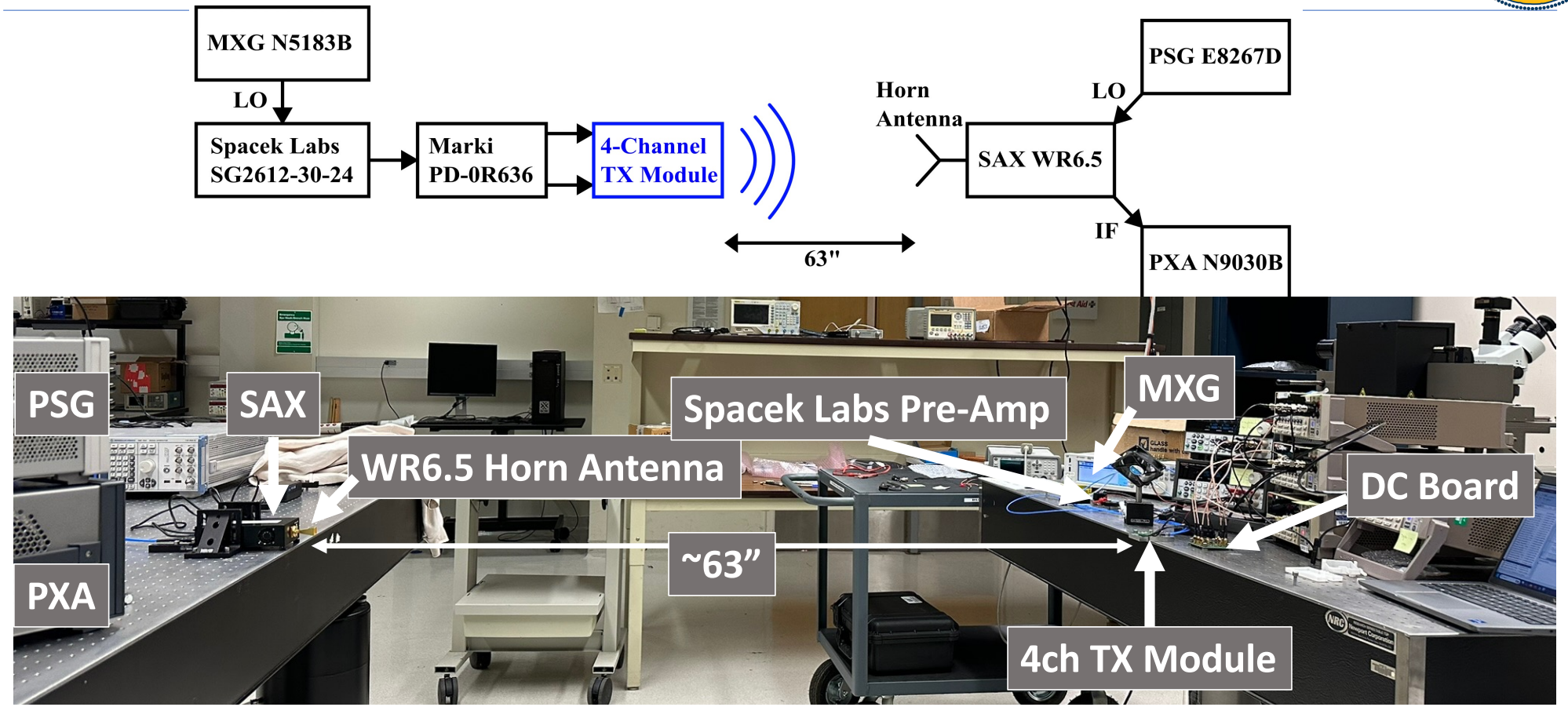
D-band Front-end Circuitry for Scaled Aperture

- Given compact circuitry
- Packaging for D-band uses LTCC substrates with Vivaldi ”slat” antennas
- Each slat consists of 4 antennas driven by a single serial IO line.



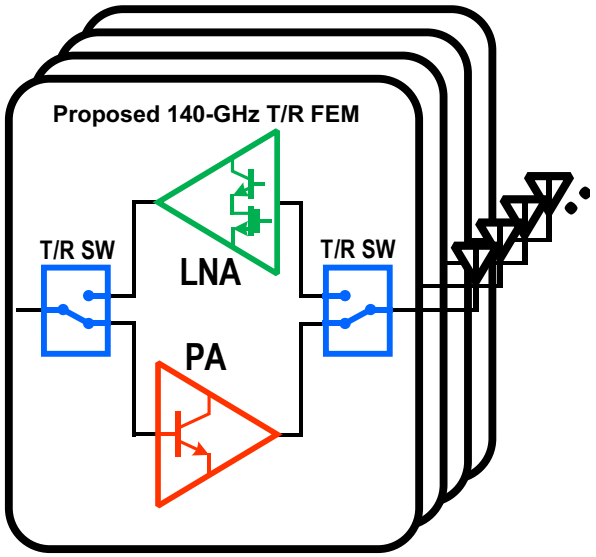
Ref: A. Dinkelacker et al., “An Antipodal SIW-fed Vivaldi Antenna at D-Band in LTCC for Flip-chip RFIC Integration,” to be presented at IMS 2025

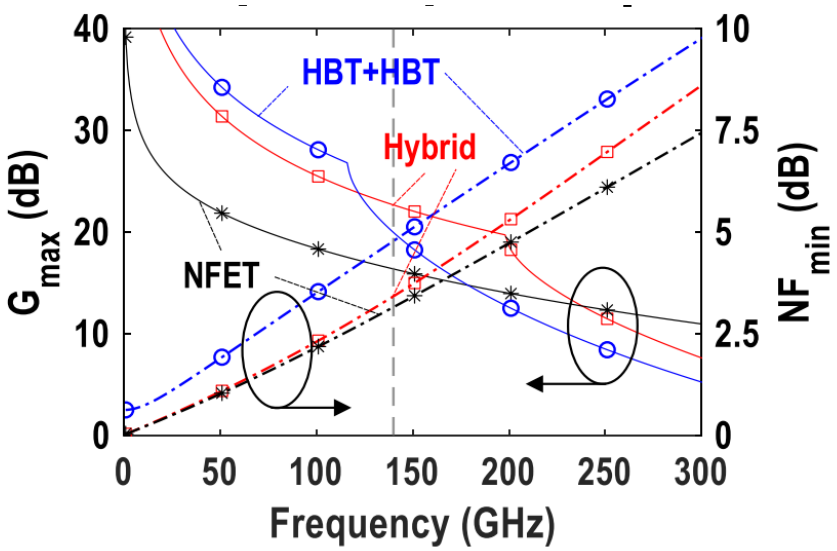
Over-the-Air Measurements



140-GHz RF Front-end Circuit

- Phased array for 140-GHz backhaul communication link
  - Antenna spacing <λ/2 = 1mm @ 140-GHz
  - Relatively poor RF performance from circuit perspective

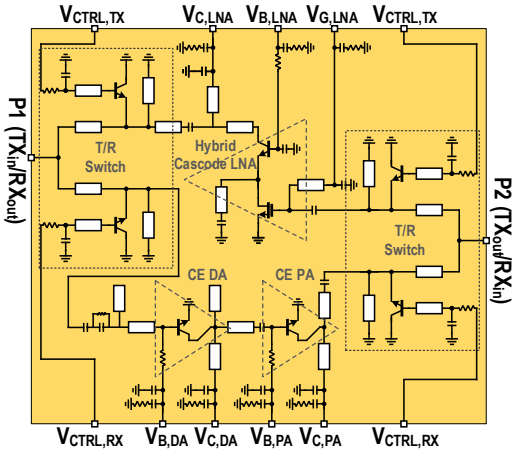


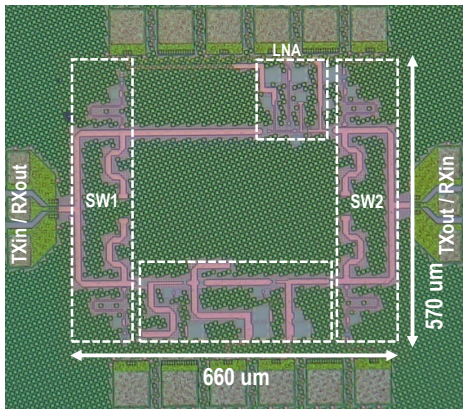


- 45-nm BiCMOS process offers both high-speed CMOS and HBT;
  1) 45-nm SOI CMOS devices (fmax = 400 GHz
  2) 90-nm HBT device (fmax = 600 GHz)

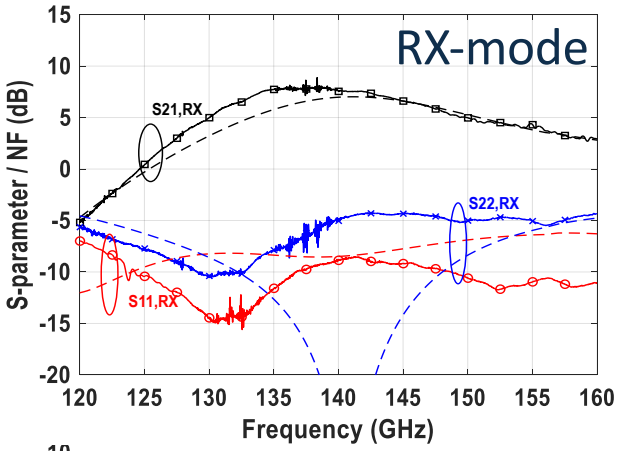
- Consider front-end integration for 100+ GHz bands

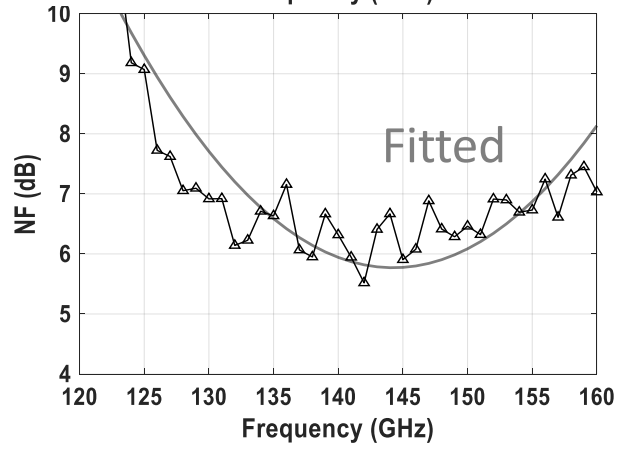
45-nm SiGe Measurements: FE RX/TX

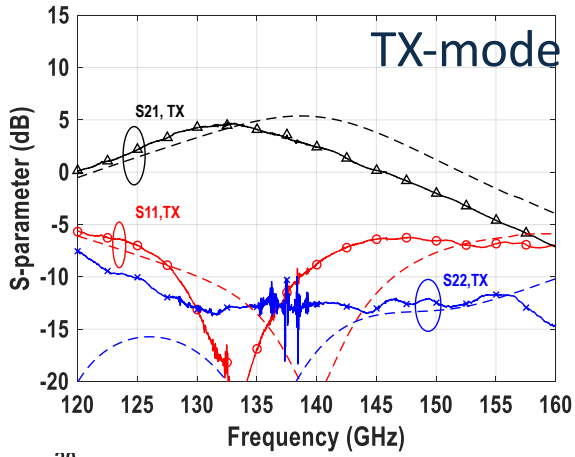


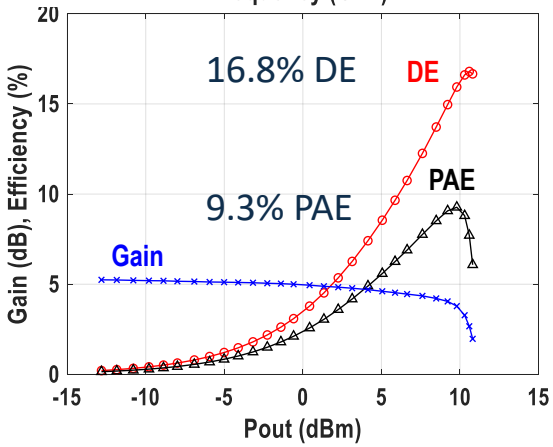


Ref: W. Lee et al., BCICTS 2024









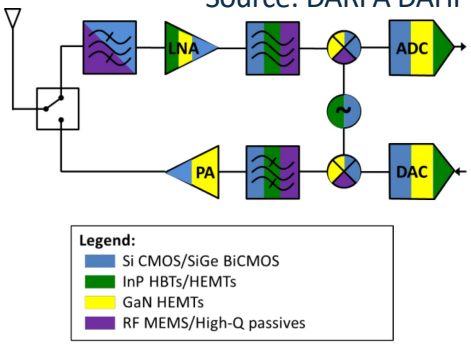
Heterogeneous Integration for T/R Front-ends

Heterogeneous Integration for 6G Front-ends

- PseudolithIC is commercializing a technology that allows the designer to mix and match any transistors into common silicon platform. Optimized RF and mixed-signal chipset solutions:

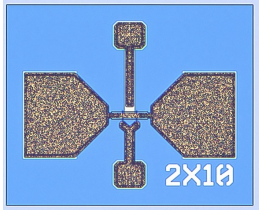
1. Silicon cost and scalability
2. X+CMOS

Source: DARPA DAHI



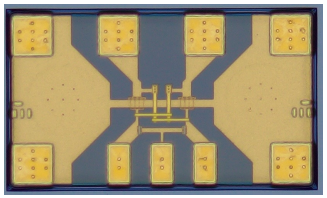
InP HEMT:

Low Noise



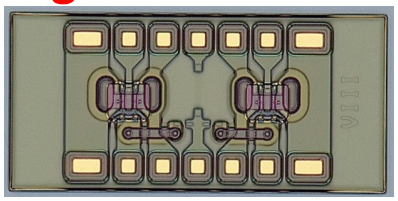
InP HBT

High Efficiency



GaN HEMT:

High Power



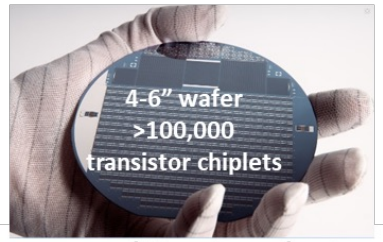
Pseudolithic Integration Process

Existing Ecosystem

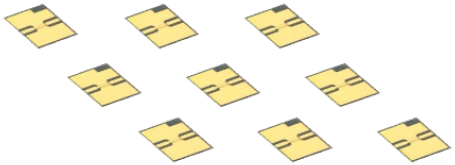
PseudolithIC Design Tools

PseudolithIC Integration Fab

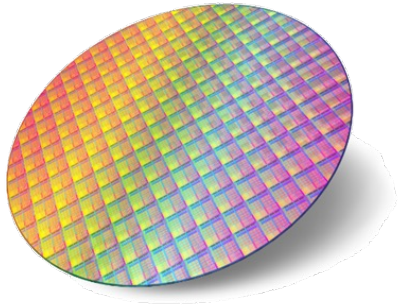
PSEUDOLITHIC Wafer
Reconstructed III-V wafers (8”)

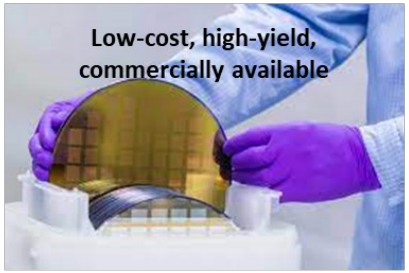


Compound Semiconductor Foundry

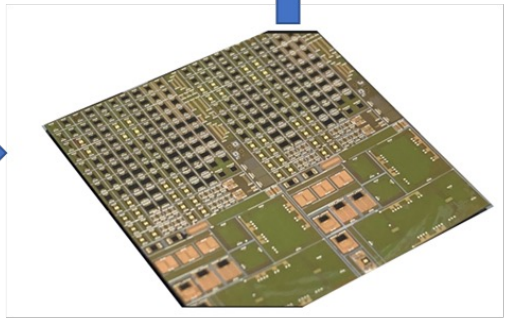


Chiplet Integration



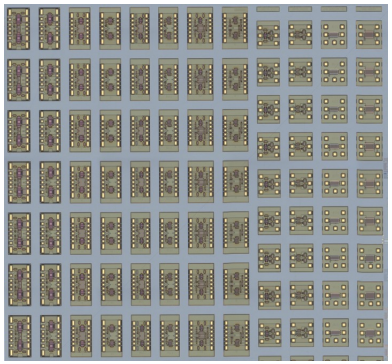


Silicon Foundry

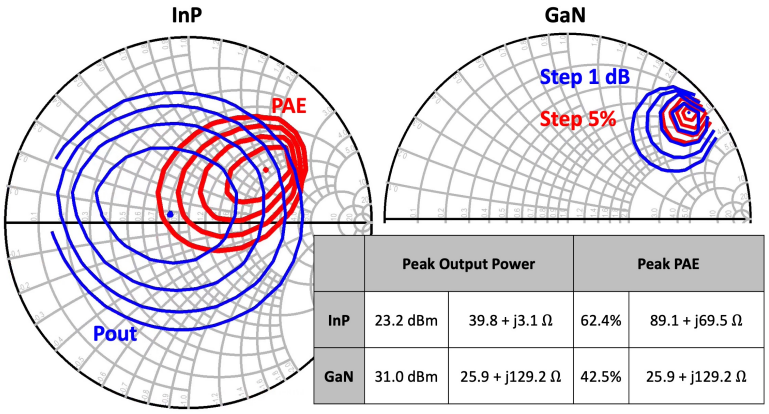


Wafer/panel level direct interconnect process on restructured wafer/panel

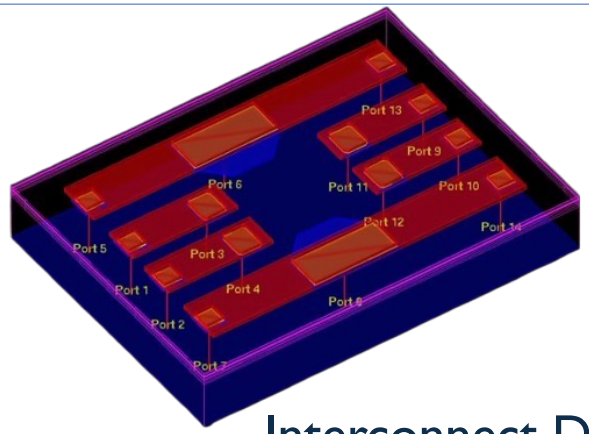
Pseudolithic Design Flow



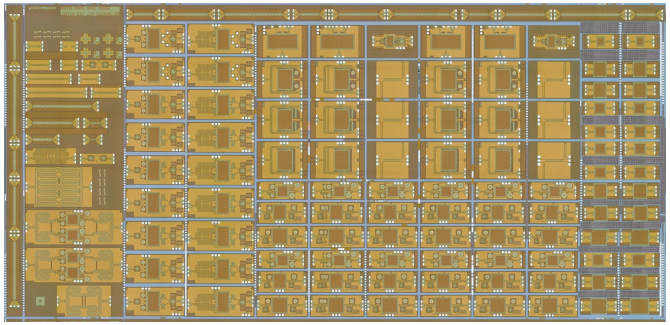
Chiplet Design



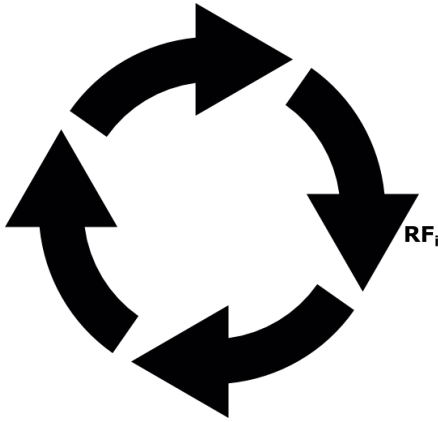
	Peak Output Power		Peak PAE	
InP	23.2 dBm	39.8 + j3.1 Ω	62.4%	89.1 + j69.5 Ω
GaN	31.0 dBm	25.9 + j129.2 Ω	42.5%	25.9 + j129.2 Ω

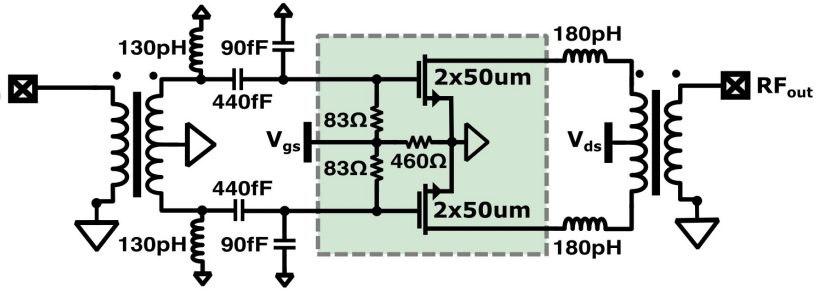


Interconnect Design



CMOS Interposer Design

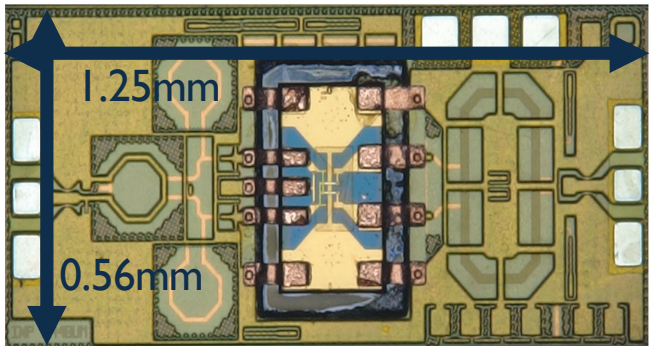


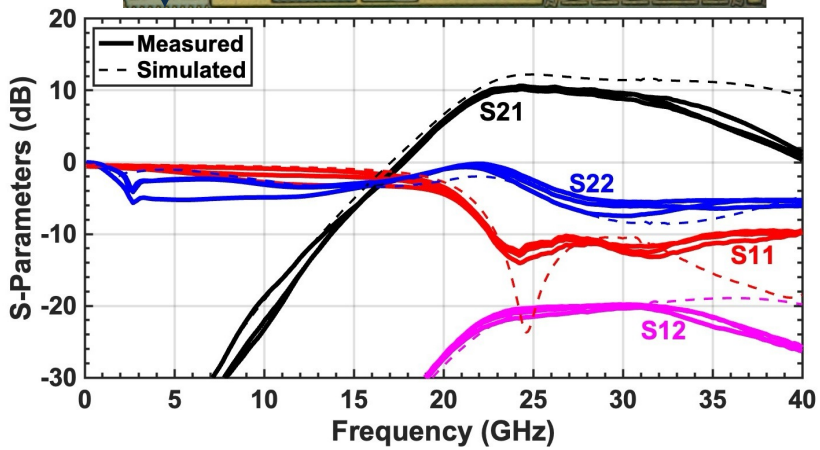


Schematic Design

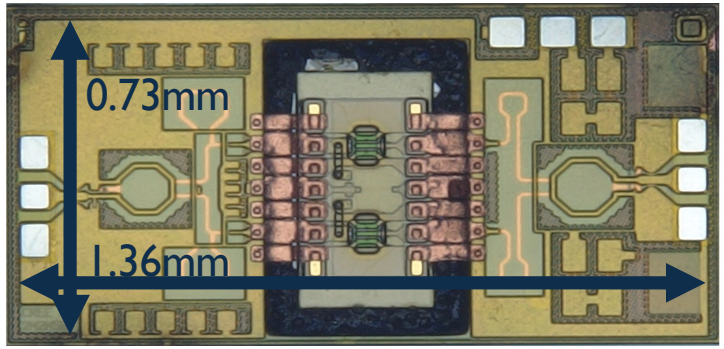
InP (left)/GaN (right) Characterization

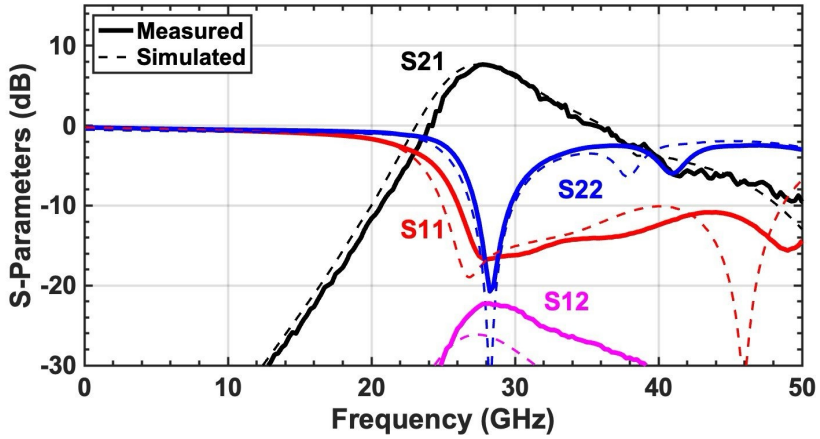
- Peak gain of 10.9 dB @ 24 GHz
- More than 35% PAE





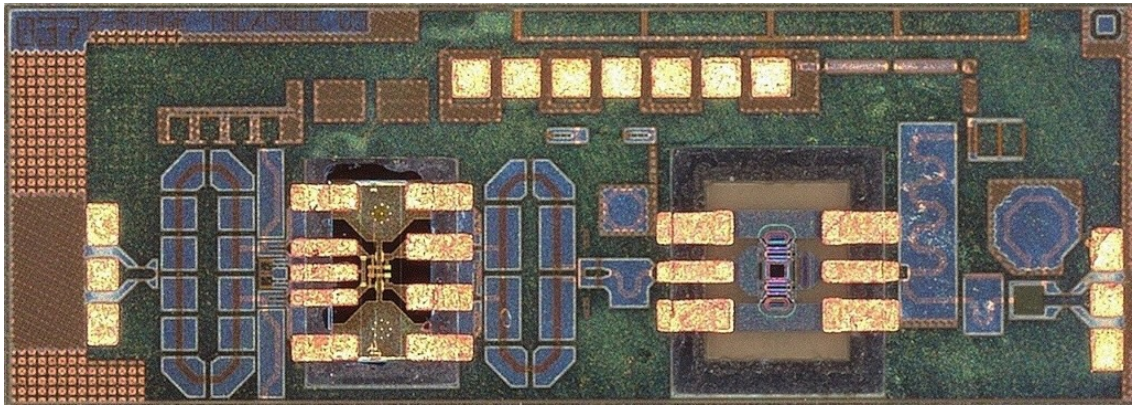
- Peak gain of 7.7 dB @ 28GHz
- 20V / 26mA quiescent bias



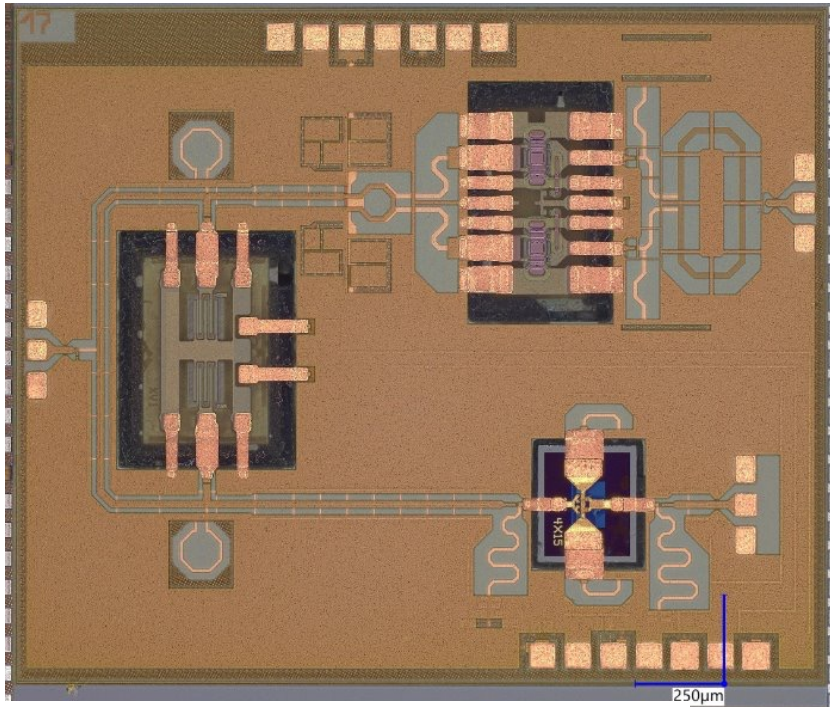


Mix and Match Technology for Millimeter-wave

- InP HBT + GaN HEMT IC Amplifier
- InP HEMT + GaN HEMT Transmit/Receive

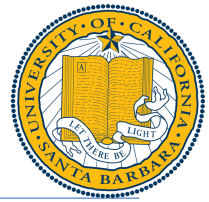


Measured over 20dB of gain at 25.7 GHz



- Developing E-band solutions with better performance than silicon at lower power consumption than GaAs!

6G Outlooks for Device Technologies



- New device technologies will impact applications & frequency bands for 6G
  - Advanced CMOS/SiGe processes will add with multifunctional arrays
  - Higher power from GaN technologies can solve mm-wave margins
- Better efficiency: SiGe and SOI technologies push to higher frequencies
- Digital at the antenna on large scales
- Improved Packaging Cost:
  - LTCC for > 100 GHz array integration
  - SOI CMOS Photonics for lightwave modes of operation
- Wafer-scale integration methods for the next generation: Integrating InP and GaN into 6G Front-ends

Acknowledgments

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- National Science Foundation (NSF) for support under the 4D100 Program
- GlobalFoundries for access to the 22FDX/45CLO/9HP (N. Cave)